



安捷倫科技高頻元件量測研討會

時間: **2006年 2月23日**

地點: **高雄金典酒店**



Agilent Technologies

Packaging Development Trend of Integrated Analysis

Sung-Mao Wu



Outline

Development Trend for PKG

- PKG Technology Trend
- Why SiP and POP/PIP

Challenges to PKG Integrity Design

- Design Challenges on Simulation, Measurement and Design
- Case I : Effective DK
- Case II : Impedance Control verify by TDR
- Case III: TDR FA Application
- Case IV : Substrate Ball Pad Design
- Case V : PDS Analysis

Integrated Design

- Components of Optimization PKG Design
- Advanced PKG Analysis Flow
- Plan and Actions for PKG Design

Interesting Semiconductor World

Fab/fabless

Copper wafer

Low K material

12" wafer

Nano meter tech

Semiconductor Industry

Front/Back end solution

Environment friendly

Compact Size

Low power consumption

Bio tech / New form chip

IC/module/System Design

High speed/high frequency

High thermal / Stress solution

Integrated System

Low cost

Short Time to Market

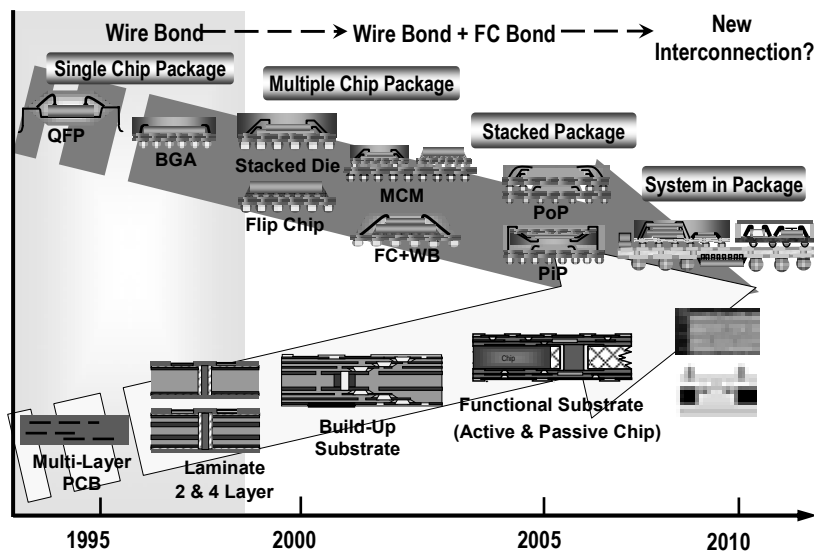
Worldwide strategy

Page 3

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Packaging Technology Trend



Page 4

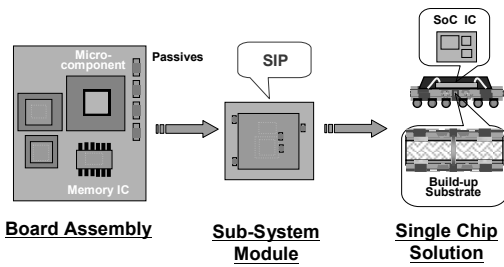
 **Aplicor Technologies**

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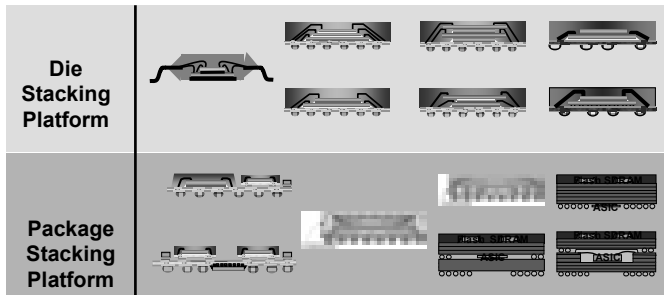
Why SIP ?

Compare to Board Assembly:
Performance Enhancement
Thinner, Smaller, and Lighter
Low Cost

Compare to SOC
Low Cost
Time to Market
Flexible



SIP Platform

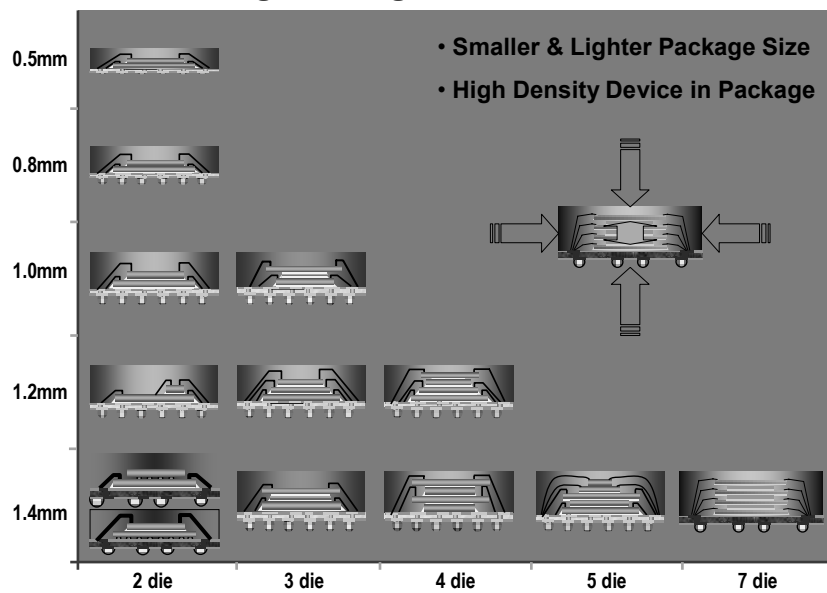


Page 5

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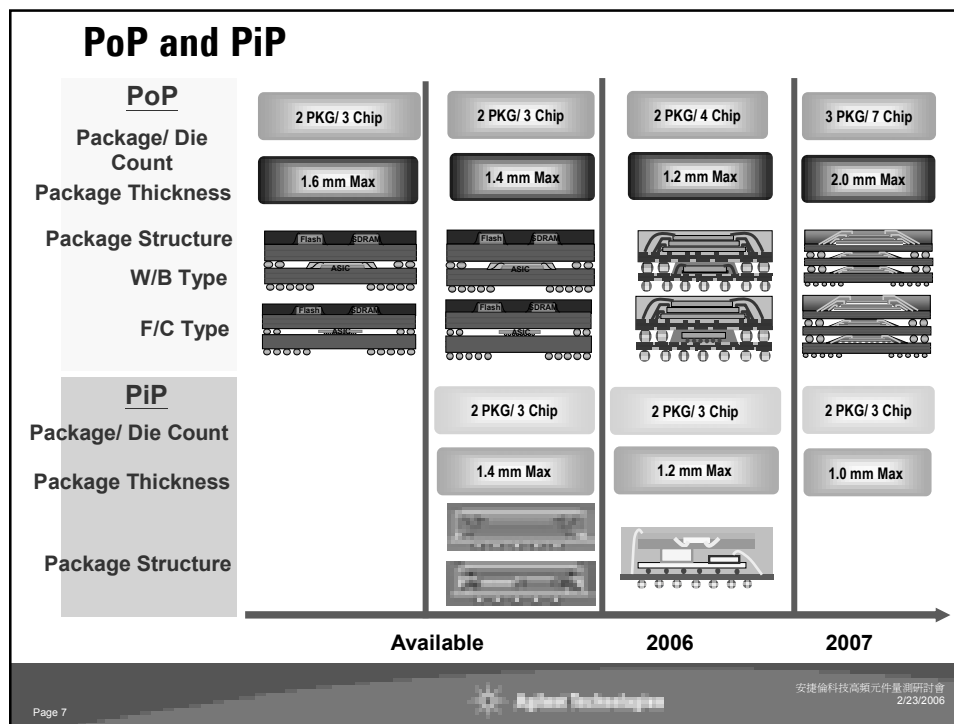
Die Stacking Package Trend



Page 6

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Fine Pitch Wire Bonding

IC Feature Size (um)	0.25	0.18	0.13	0.09	0.065
• Wire Bond pad Pitch (um) (Single-In-Line)	 60	50	45	40	35
• Wire Bond Pad Pitch (um) (2 Row Staggered)	 80/40	70/35	60/30	50/25	40/20
• Wire Bond Pad Pitch (um) (Tri-Tier)	 90/45	80/40	70/35	60/30	50/25
• Wire Bond pad pitch (um) (Quad-Tier)	 100/50	90/45	80/40	70/35	60/30

■ Leading-Edge Fine-Pitch Capabilities

- In-Line: 45 um; Staggered: 60 um; Tri-Tier: 70 um ; Quad-Tier: 80um

■ Low k & Copper wafer capabilities available.



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Trends of Packaging Technologies

- Focus Packages - Bumping, WLCSP, FCBGA, SIP, SCSP and modified LF package
- Small & Light
 - Thin Thickness in Wafer, Substrate, Package
 - Fine Pitch in Wire Bonding, Flip Chip Bond and Solder Ball
 - High Density by Stacked Die, Package, Multi-Substrate Layer, Substrate Stacked, Staggered Via and Small Trace Via Hole Size
- Good Thermal and Electrical Performance
 - High Speed and Low Thermal Resistance
 - Cu / Low-K wafer, Nano-technology
- Green
 - Green Solution
- Low Cost & Fast Time-to-market
 - 12" Wafer Capacity
 - Total Turnkey Solution
 - Matrix design, Multi-die, package Design
 - LAB Design Support

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Integrated Design

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- Plan and Actions for PKG Design

Challenges to PKG Integrated Design

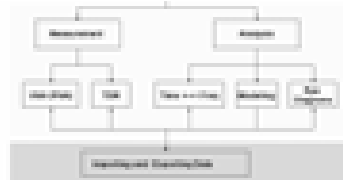
Analysis Challenges

- Multi-port parameters analysis and broadband calibration skill
- Double-side calibration and probing technology
- Signal-integrity, SSN/SSO and IP drop
- Mixed-signal analysis
- Substrate On-line testing, like via, bump and ball.....



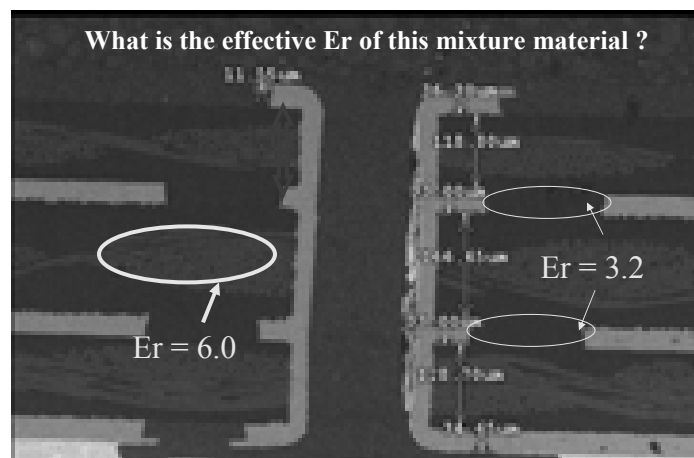
Design Challenges to SiP

- PKG selection for different thermal/electrical request
- Substrate Design integrated thermal/electrical solution.
 - Embedded Die/passive, IPD, decoupling cap.....
- PKG IP development.
- Design Guideline and constraint



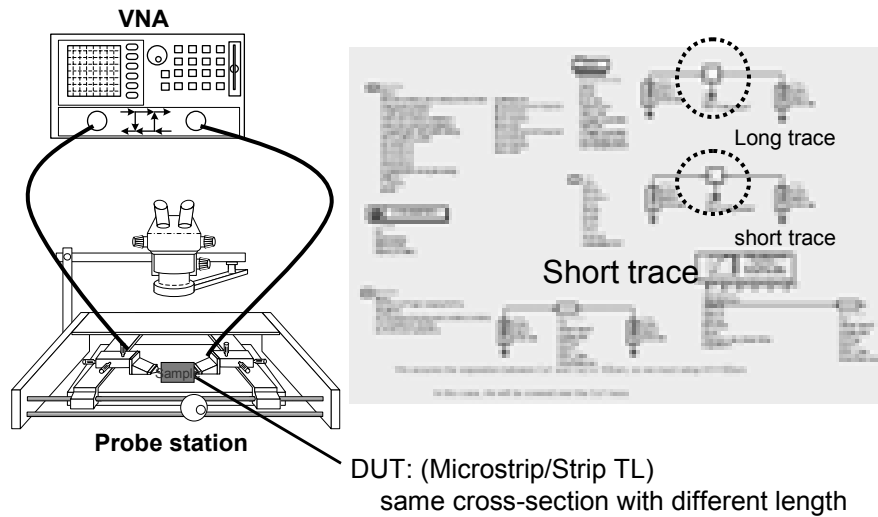
Analysis Case I :

→ effective dielectric constant



Analysis Case I :

→ Measurement and ADS setup



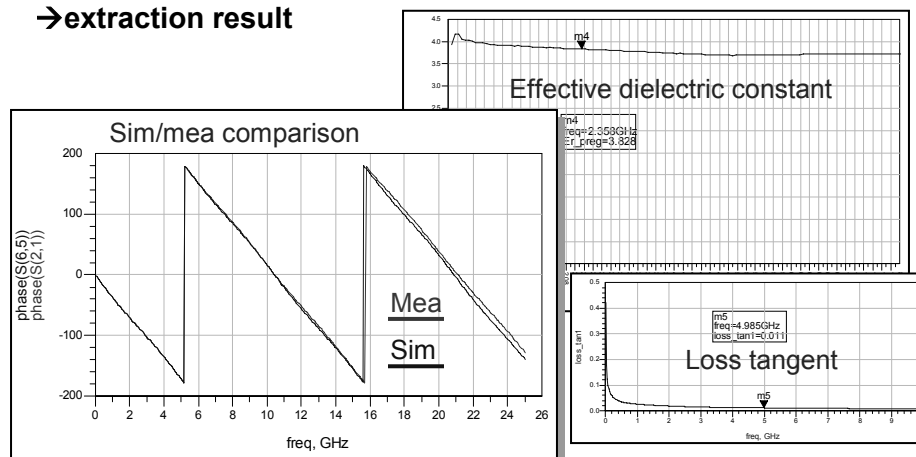
Page 13

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Analysis Case I :

→ extraction result



Good Correlation between simulation and measurement

Once we have the accurate the dielectric constant of mixture material of substrate, we can achieve good electrical substrate design.

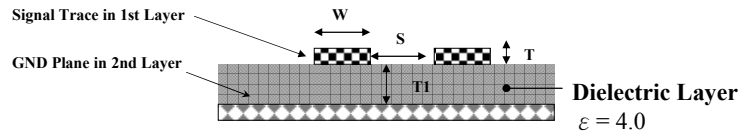
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Analysis Case II :

→ Impedance Control Verify by TDR/TDR System



Design Condition:

Substrate Type : 2 Layer

Impedance Control : Differential

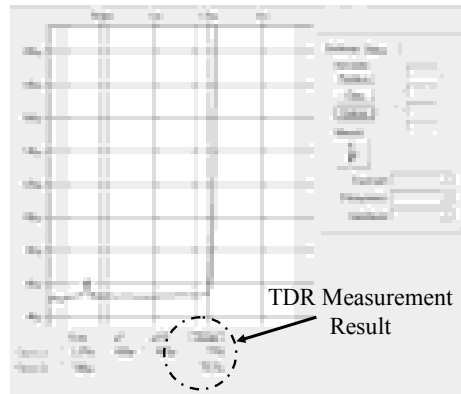
Simulation Structure : Micro-Strip Line

Trace Width (W): 0.39mm

Trace Thickness (T): 22 μm

Dielectric Thickness (T1): 200 μm

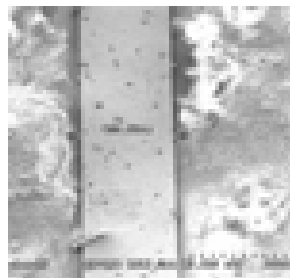
Separation (s): 0.15mm



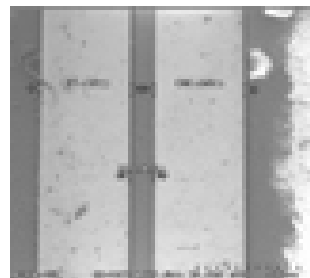
Impedance Control

-- Manufacture Result and comparison

**SEM-single ended trace
width measurement**



**SEM-differential trace
width/space measurement**

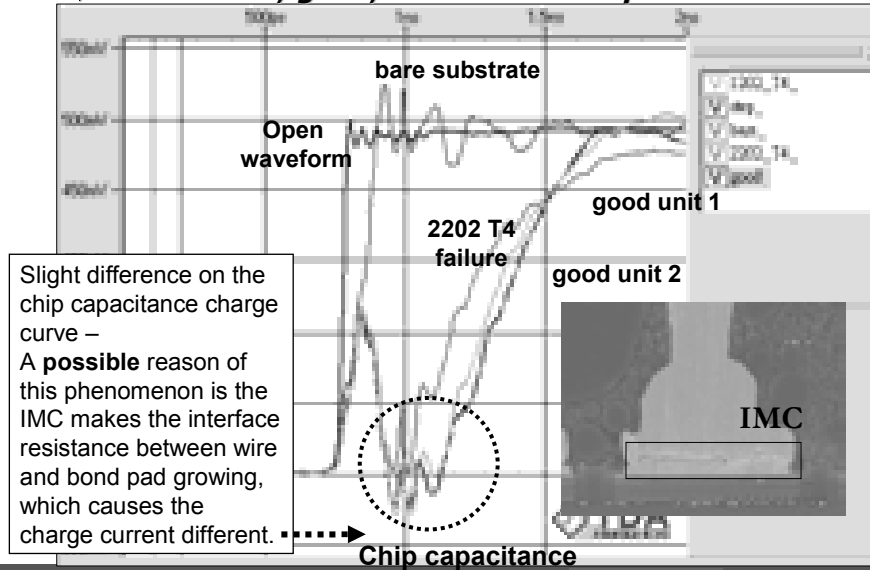


Design / Measurement Comparison

	Impedance comparison				
	Trace width(μm)	separation(μm)	Zodd(ohm)	Zeven(ohm)	Single ended(ohm)
Q2D	388.95(from drawing)	150(from drawing)	41.2	58.8	50.9
Q2D	429 μm	116 μm	38.1267	55.6689	47.5768/435 μm
TDR	429 μm	116 μm	42.4~42.8	61.7	52.3~53

Analysis Case III →FA Application

▼TDR of bare, good, and failure sample



Page 17

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Analysis Case IV :

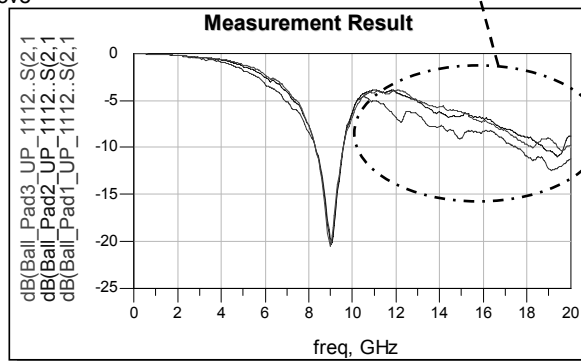
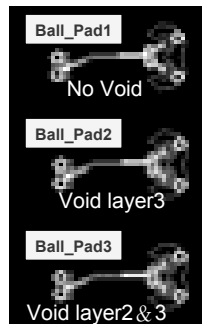
→Ball pad effect analysis



Void PWR/GND plane above the ball land on Layer3



Void the plane above ball pad area at PWR/GND will reduce the capacitance,

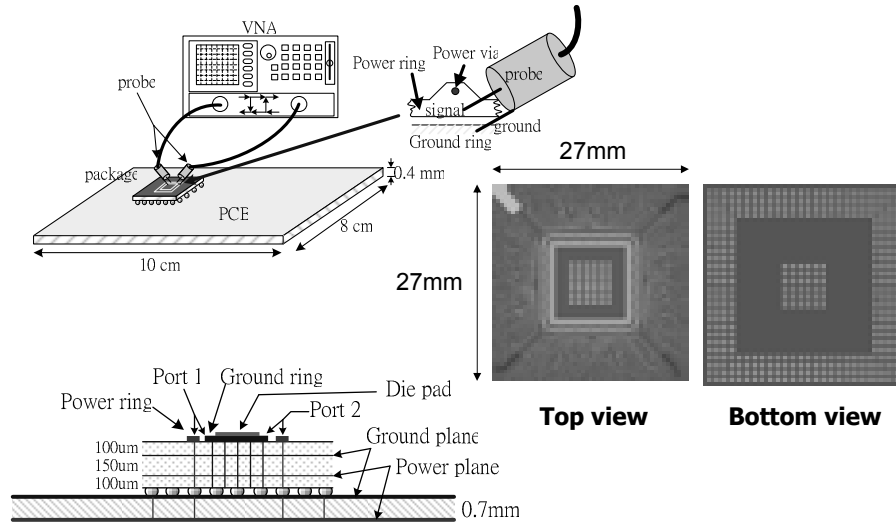


Page 18

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Analysis Case V : PDS Analysis -- Measurement setup



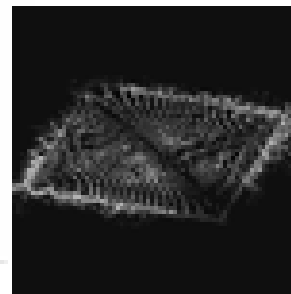
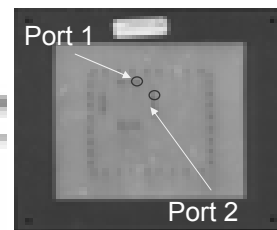
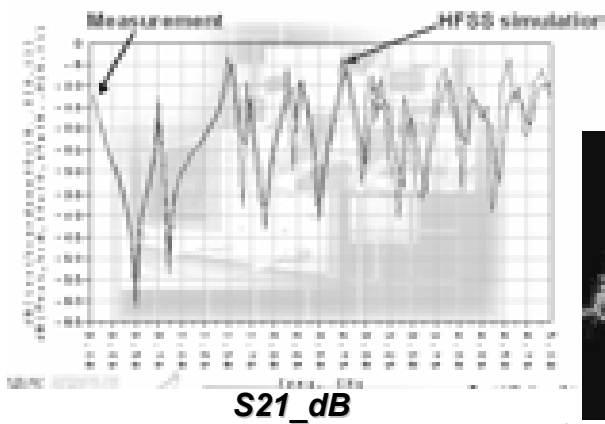
Page 19

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Analysis Case V : → Measurement and Simulation Result (Test Board only)

Correlation between measurement and simulation



Field propagation @750MHz

Page 20

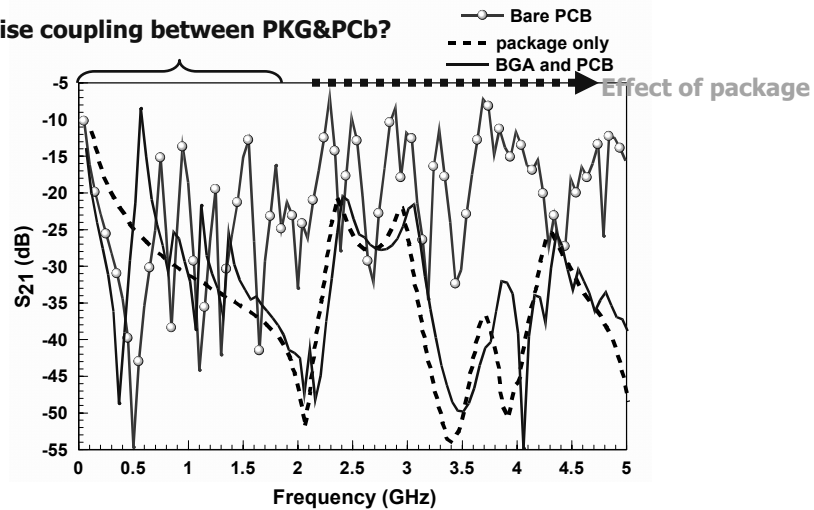
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Analysis Case V :

→ comparison with bare PCB, Package and BGA+PCB

Noise coupling between PKG&PCB?



Page 21



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Integrated Design

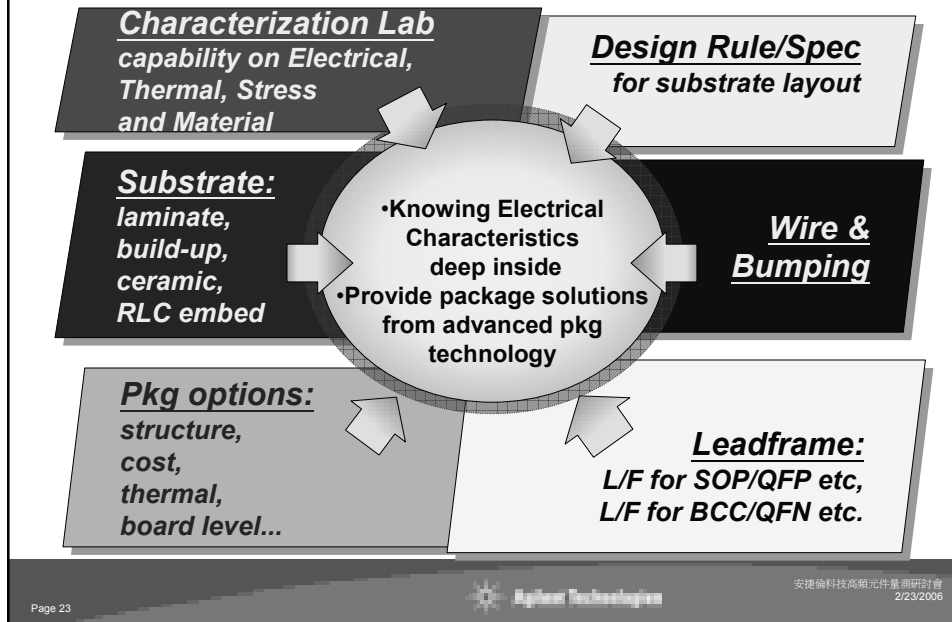
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Page 22

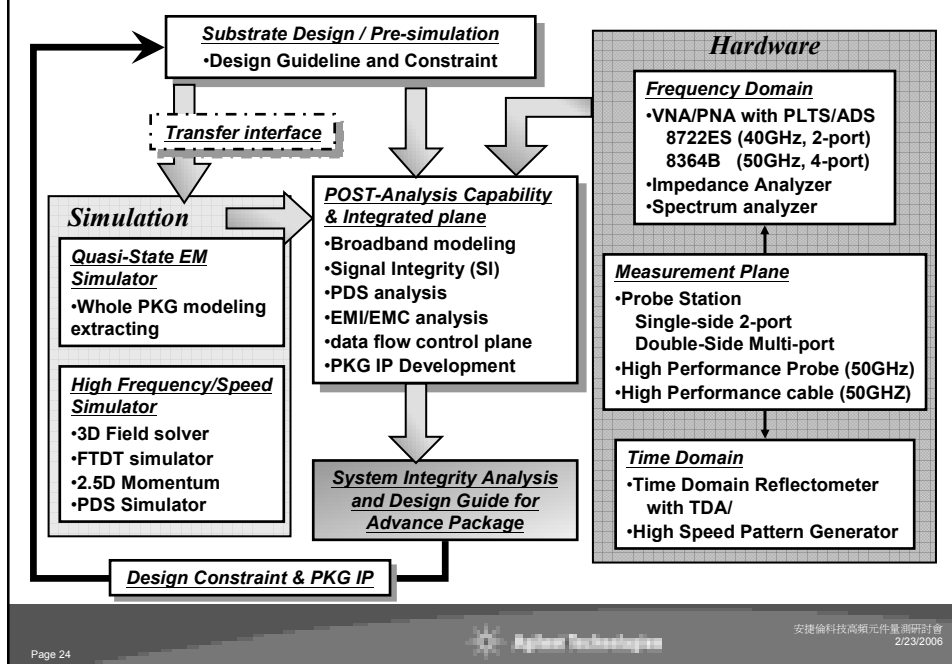


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Components of Optimization Package Design



Integrity Design Flow for Advanced PKG



Plan and Actions for PKG Design

- ▲ Substrate Design Integrity Electrical Performance
 - Design Integrity Electrical performance flow
 - Design Rule and Constraint setting for SiP PKG Application, like RF Module, optical and wireless PKG
- ▲ Active/Passive Device analysis capability
 - Embedded passive (RF-MEMS, Substrate embedded RLC) analysis and IP-development
 - Sub-system measurement capability setting for advanced PKG
- Co-Design and Co-development with key partners
- ▲ -Co-working with key partners for more close and detail study in Wireless, Optical or RF module

Contacts

- Samuel_Wu, Leader of Electrical Lab
E-mail: samuel_wu@aseglobal.com
Phone: 886-7-3617131 ext. 15290/85290
Fax: 886-7-3613094
- Mark_Li, Project Engineer of Electrical Lab
E-mail: Mark_li@aseglobal.com
Phone: 886-7-3617131 ext. 15291/85291
Fax: 886-7-3613094

ASE, Inc (Kaohsiung)
26, Chin 3rd Rd.,
811, Nantze Export Processing Zone
Kaohsiung, TAIWAN

Website: www.aseglobal.com

THE END

Thank You For Your Listening



ASE GROUP
日月光集團

PNA Based Solutions

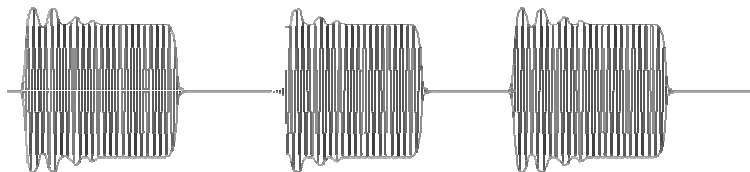
- Pulsed RF S-Parameter Measurements
- Multiport Test Solutions
- Physical Layer Test Systems

Agilent Technologies Ltd.

Ming-Fan, Tsai
Project Manager

Feb, 23, 2006

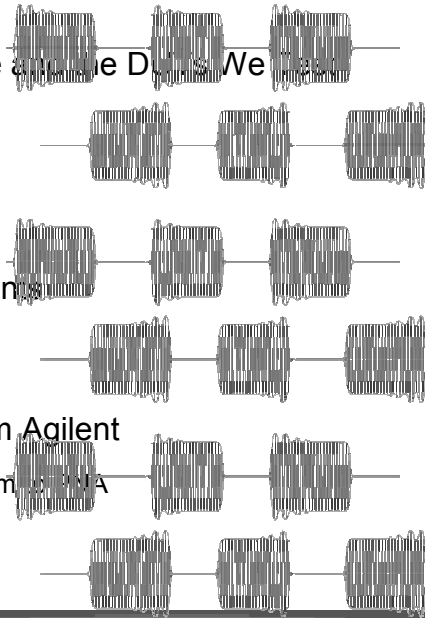
Pulsed-RF S-Parameter Applications Using The Agilent PNA Series Network Analyzer



Agenda

→ Why Measure in Pulsed Mode and the DUTs We Test

- Wafer Test
- Power Amplifiers
- Antenna RCS
- T/R Modules
- Review of Pulsed Measurements
 - Wideband synchronous
 - Narrowband asynchronous
- Evolution of Pulsed VNAs from Agilent
 - 8510, 85108, 85120, CTS Platform VNA
- Test Sets Available



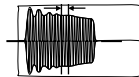
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Why Test Under Pulsed Conditions?

- **Device may behave differently between CW and pulsed stimuli**
 - Bias changes during pulse might affect RF performance
 - Overshoot, ringing, droop may result from pulsed stimulus
 - Measuring behavior within pulse is often critical to characterizing system operation (radars for example)
- **CW test signals would destroy DUT**
 - High-power amplifiers not designed for continuous operation
 - On-wafer devices often lack adequate heat sinking
 - Pulsed test-power levels can be same as actual operation



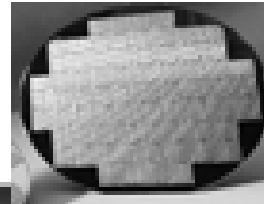
Page 4

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On-Wafer Amplifier Test and Modeling

- Most applications are at microwave frequencies
- Devices lack adequate heatsinking for CW testing, so pulsed-RF used as a test technique to extract S-parameters
- Arbitrary, stable temperature (isothermal state) set by adjusting duty cycle
- Duty cycles are typically $< 1\%$
- Often requires synchronization of pulsed bias and pulsed RF stimulus



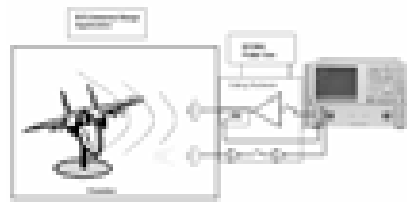
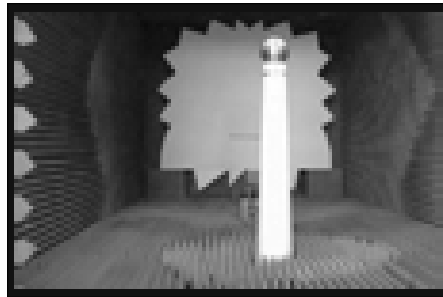
Wireless Communications Systems

- TDMA-based systems often use burst mode transmission
 - Saves battery power
 - Minimizes probability of intercept
- Power amplifiers often tested with pulsed bias
- Most of wireless communications applications ≤ 6 GHz



Pulsed Antenna Test

- About 30% of antenna test involves pulsed-RF stimulus
- Test individual antennas, complete systems, or RCS
- RCS (Radar Cross Section) measurements often require gating to avoid overloading receiver



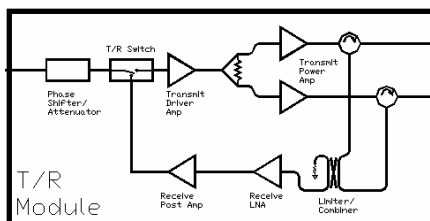
Page 7

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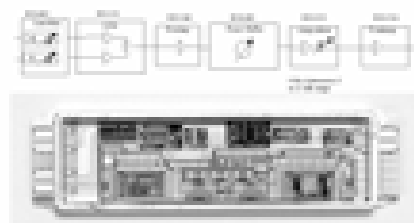
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Component-Level Characterization

- Accurate characterization of components such as amplifiers, mixers, filters, and antennas is critical for effective system simulation
- Pulsed-RF stimulus crucial for many components in A/D applications such as AESA Phased arrays and the individual T/R Modules that are used in such systems



Transmit / Receive Module



Receive Module

Page 8

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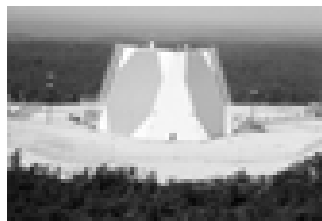
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Radar and Electronic-Warfare

- Biggest market for pulsed-RF testing
- Traditional applications ≤ 20 GHz
- Many now include Multi-Mode Ka-Band
- Devices include
 - amplifiers
 - T/R modules
 - up/down converters



AN/APG-79 F16C Block 60



Pave-Paws



AN/APG-81 JSF

Agenda

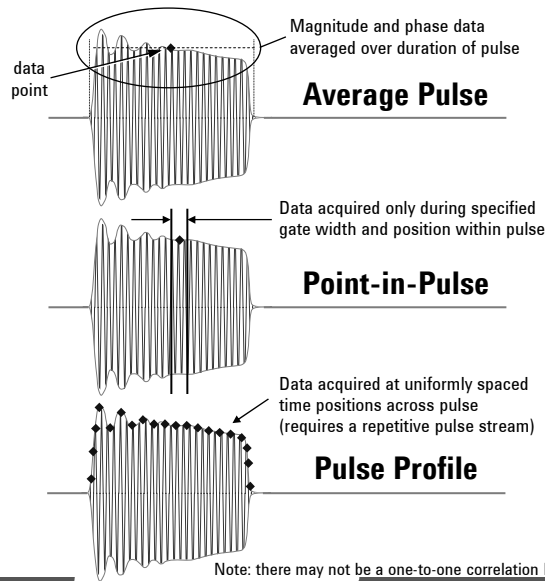
- Why Measure in Pulsed Mode and the DUTs We Test
 - Wafer Test
 - Power Amplifiers
 - Antenna RCS
 - T/R Modules



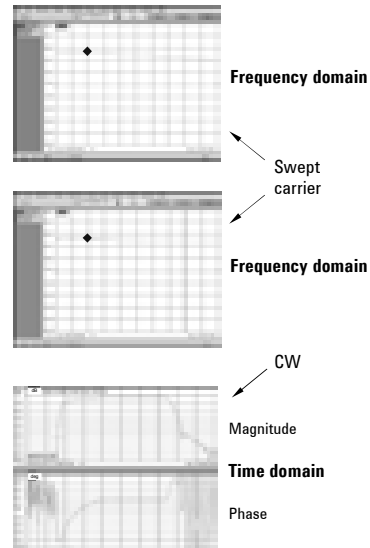
Review of Pulsed Measurements

- Wideband synchronous
- Narrowband asynchronous
- Evolution of Pulsed VNAs from Agilent
 - 8510, 85108, 85120, CTS Platform, PNA
- Test Sets Available

VNA Pulsed-RF Measurements

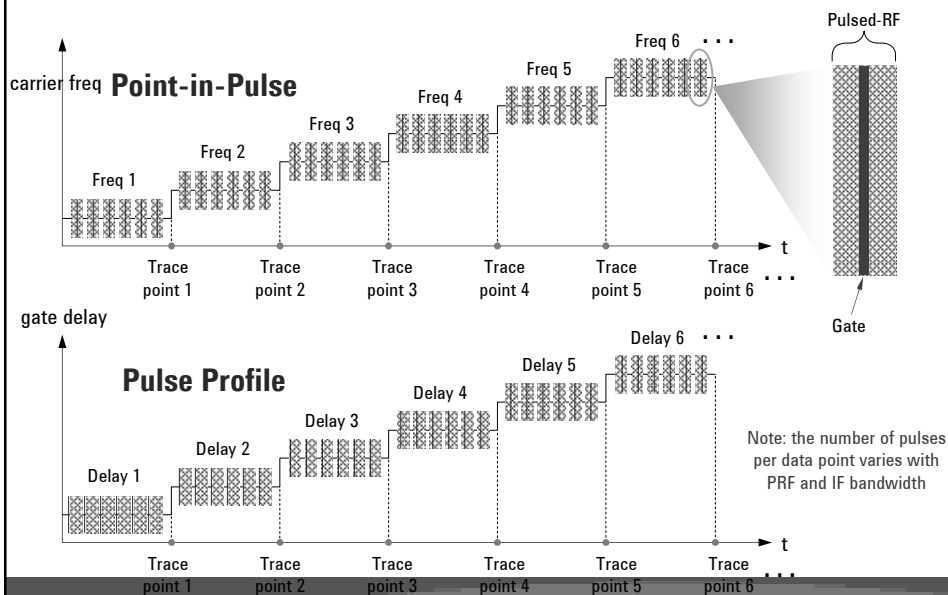


VNA data display



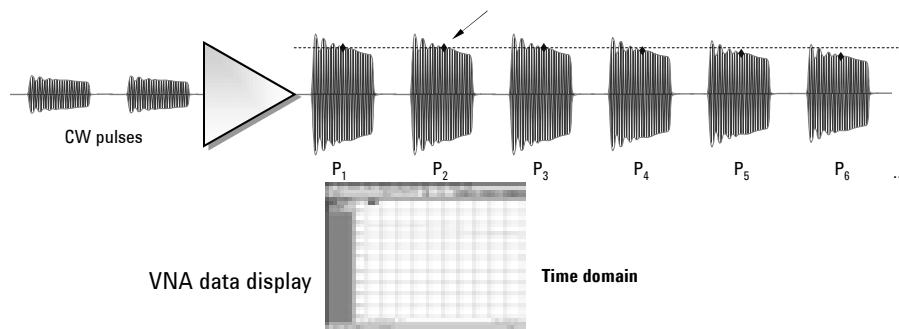
Note: there may not be a one-to-one correlation between data points and the actual number of pulses that occur during the measurement

Pulsed-RF Data Acquisition (Time Domain View)



Pulse-to-Pulse (Single Shot) Measurements

- Carrier remains fixed in frequency
 - Measurement point in pulse remains fixed with respect to pulse trigger (requires wideband detection technique)
 - One data point for each successive pulse, no pulses skipped
 - Display magnitude and/or phase versus time
- One data point for each successive pulse, no pulses skipped



Page 13

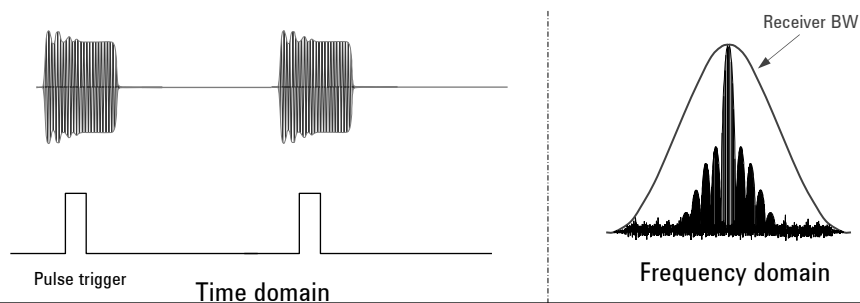
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Pulsed S-parameter Measurement Modes

Wideband/synchronous acquisition

- Majority of pulse energy is contained within receiver bandwidth
- Incoming pulses and analyzer sampling are synchronous (requires a pulse trigger, either internal (8510) or external (PNA))
- Pulse is "on" for duration of data acquisition
- No loss in dynamic range for small duty cycles (long PRI's), but there is a lower limit to pulse width



Page 14

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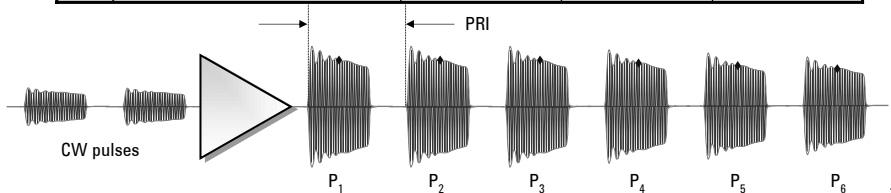
Minimum Pulse Widths for Point-in-Pulse Measurements Using Wideband Detection

	Maximum IF bandwidth	Minimum pulse width	IF auto-gain mode*
PNA models (20, 40, 50, 67 GHz)	40 kHz	50 us	Yes
PNA-L models (2-port, 20, 40, 50 GHz)	250 kHz	10 us	Yes
PNA-L models (2-port, 6, 13.5 GHz; 4-port, 20 GHz)	600 kHz	2 us	No

* Note: for point-in-pulse measurements, the IF auto-gain mode should be turned off (i.e., set IF gains manually)

Fastest PRI/PRF for Pulse-Pulse Measurements Using Wideband Detection

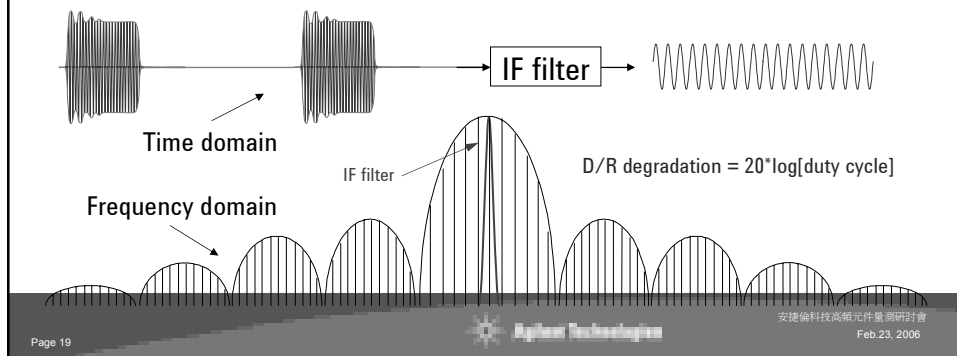
Conditions: point sweep; external trigger, CW sweep; IF autogain=off	Maximum IF bandwidth	Minimum PRI	Maximum PRF
PNA models (20, 40, 50, 67 GHz)	40 kHz	170 us	5.9 kHz
PNA-L models (2-port, 20, 40, 50 GHz)	250 kHz	80 us	12.5 kHz
PNA-L models (2-port, 6, 13.5 GHz; 4-port, 20 GHz)	600 kHz	40 us	25 kHz



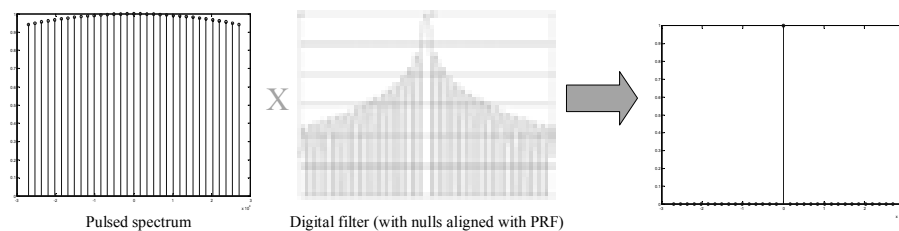
Pulsed S-parameter Measurement Modes

Narrowband/asynchronous acquisition

- Extract central spectral component only; measurement appears CW
- Data acquisition is not synchronized with incoming pulses (pulse trigger not required)
- Sometimes called "high PRF" since normally, $PRF \gg IF$ bandwidth
- "Spectral nulling" technique achieves wider bandwidths and faster measurements
- No lower limit to pulse width, but dynamic range is function of duty cycle



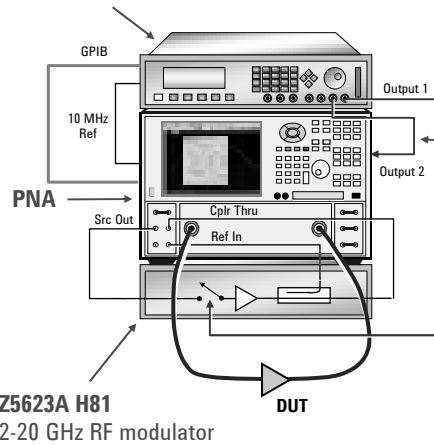
Filtered Output Using Spectral Nulling



- With "custom" filters, number of filter sections (M) can be chosen to align filter nulls with pulsed spectral components
- With spectral nulling, reject unwanted spectral components with much higher IF bandwidths compared to using standard IF filters
- Result: faster measurement speeds!

Typical Hardware Setup (Narrowband)

External pulse generator
(e.g., 81110A/81111A)



PNA (20, 40, 50, or 67 GHz) with:

- 014 Configurable test set
- UNL Source attenuators
- 080 Frequency offset mode
- 081 Reference switch
- H11 IF access
- H08 Pulsed-RF measurement capability
- 016 Receiver attenuators (optional)

Pulse 2 drive to PULSE IN B (for point-in-pulse measurements)



Page 21

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→ Evolution of Pulsed VNAs from the Past

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Page 22

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85108A

First True pulsed Network Analyser

Still the most widely used system for TR
Module R&D and manufacturing test (>100
off world-wide still in use)

Wholly COTS solution

Affordable

Low cost of ownership

Low risk

Point-on-pulse

Pulse profile, repetitive



Page 23

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Pulsed PNA is the New Generation 85108A

COTS stand alone hardware
can perform:

- Point-on-pulse
- Pulse-to-Pulse
- Pulse profile

Timing generator can trigger custom
user hardware e.g.

TR Module controller

Very much faster measurement speed



Page 24

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Comparing the 8510 and PNA 8510 (85108A)

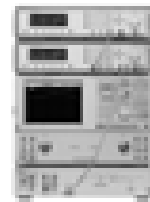
- Dominant mode is wideband detection
- Detection is done BEFORE analog-to-digital conversion
- Analog synchronous detector produces baseband I/Q output (detector bandwidth = 1.5 MHz)
- Pulse profiling achieved by varying sample point of baseband pulses
- Trade off speed and dynamic range with averaging

PNA

- Dominant mode is narrowband detection
- All processing (filtering and detection) is done digitally
- Widest bandwidth = 35 kHz
- Pulse profiling achieved with analog switches that gate IF (or RF) signals
- Trade off speed and dynamic range with variable IF bandwidths and averaging

PNA-L

- **Dominant mode is wideband detection**
- All processing (filtering and detection) is done digitally
- Widest bandwidth = 600 kHz
- Trade off speed and dynamic range with variable IF bandwidths and averaging



Agilent TR Module Test Systems

85120A S10 Family



84000A Family



Agilent TR Module Test Systems continued

CTS-I Family



CTS-II Family



Pulse Summary

	Wideband/Synchronous	Narrowband/Asynchronous
Advantages	Constant dynamic range	Narrow pulse widths
Disadvantages	Lower pulse width limit	Dynamic range loss with small duty cycles
	Elevated noise floor	No pulse-to-pulse
8510	PW > 1 us	Limited* (High PRF Mode)
PNA	PW > 50 us/10 us/2 us**	PW > 20 ns (limited by IF gate)
PNA Options	None required	H11/H08***
Measurements	Average	Average
	Point-in-pulse	Point-in-pulse
	Pulse profile	Pulse profile
	Pulse-to-pulse	

* No nulling, no point-in-pulse

** PNA/PNA-L 2-port 20, 40, 50 GHz/PNA-L 2-port 6, 13.5, 4-port 20 GHz

*** Option H08 is usually used in conjunction with Option H11. Without H11, the user can perform average pulse, or point-in-pulse measurements using external RF gates.

Agenda

• Why Measure in Pulsed Mode and the Downs We Face

- Wafer Test
- Power Amplifiers
- Antenna RCS
- T/R Modules

• Review of Pulsed Measurements

- Wideband synchronous
- Narrowband asynchronous

• Evolution of Pulsed VNAs from Agilent

- 8510, 85108, 85120, CTS Platform, VNA

→ Test Sets Available

Page 29

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Z5623A Hxx RF Modulators

• Z5623A H81 (2-20 GHz)

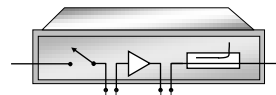
- Expected to be most common configuration (\$43K)
- Contains pin switch, amplifier, directional coupler
- Use jumpers to bypass internal amp or use high-power external amp

• Other quoted test sets:

- Z5623A H83 1-20 GHz Bidirectional (two pin switches) \$80K
- Z5623A H84 20-40 GHz Bidirectional (two pin switches) \$105K
- Z5623A H85 20-40 GHz Unidirectional, no amplifier \$35K
- Z5623A H86 2-40 GHz Unidirectional, dual band (incl. band switch) \$65K

• Customization via Agilent's "Special Handling" group:

- Different frequency ranges
- No amplifier or higher power amplifiers
- High power components



Z5623A H81

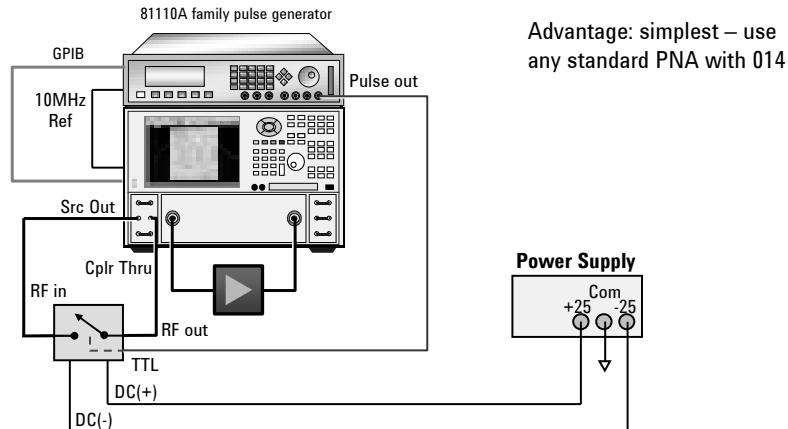
Page 30

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PNA Pulsed-RF Configuration Example 1

- User-supplied external modulator
- Average pulse measurements



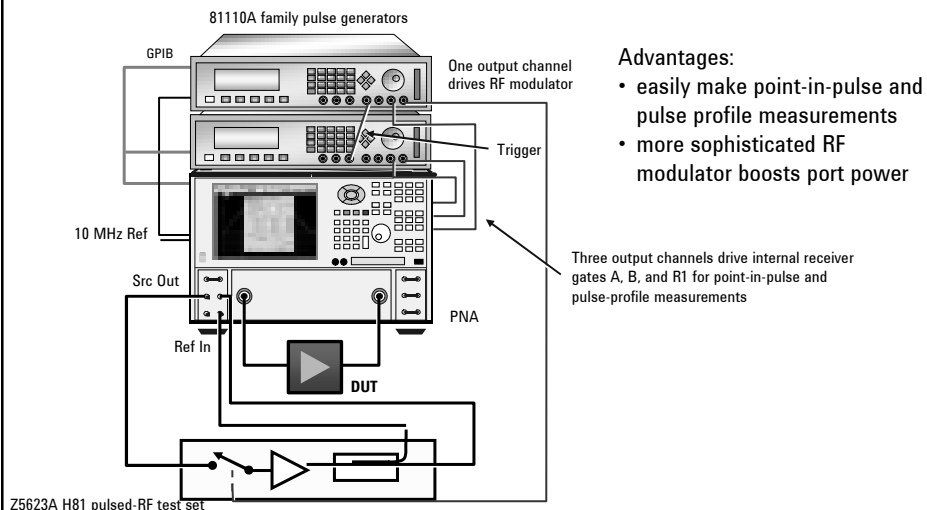
Page 31



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PNA Pulsed-RF Configuration Example 2

- Modulator test set, internal receiver gates
- Point-in-pulse, pulse profile of S21 and S11



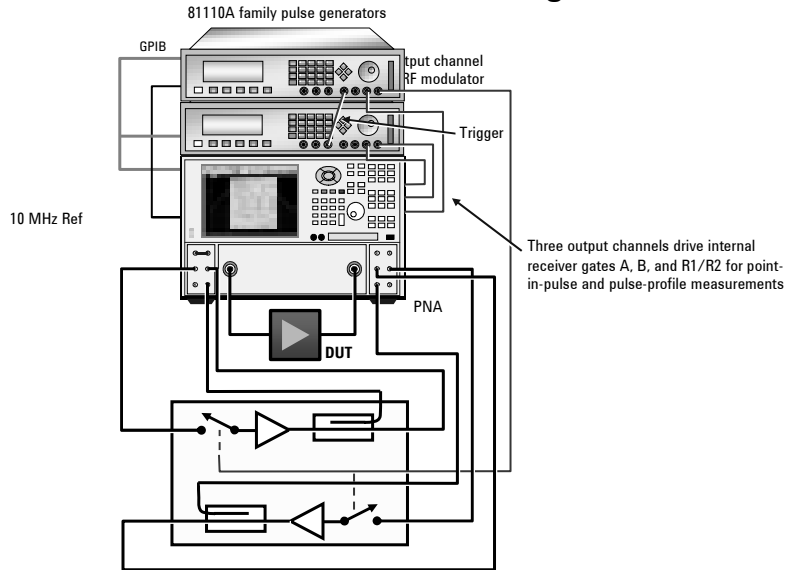
Z5623A H81 pulsed-RF test set

Page 32

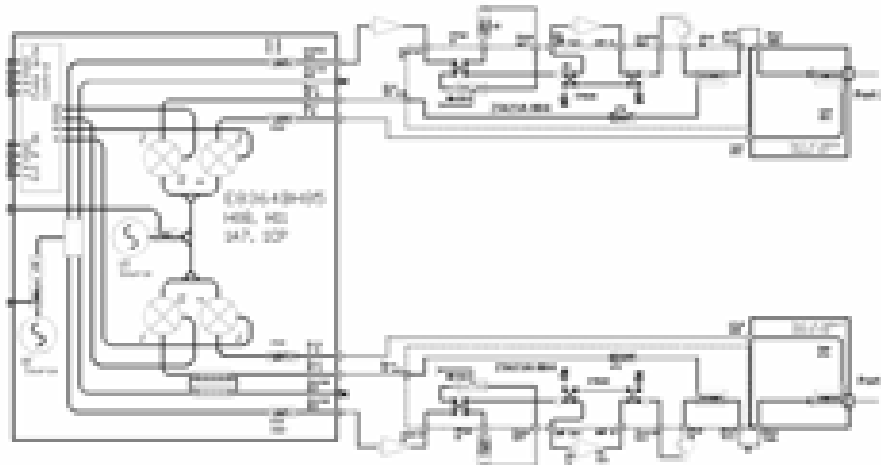


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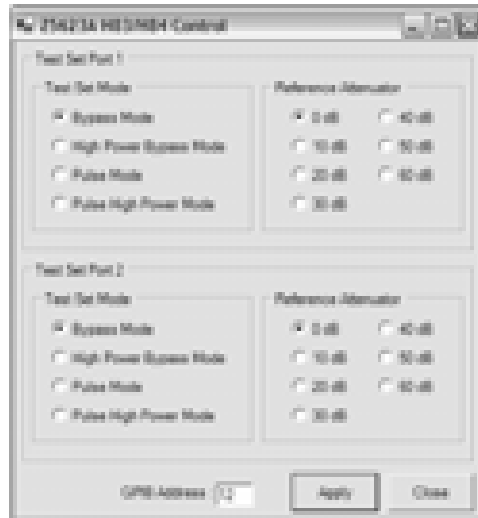
PNA Pulsed-RF Configuration Example 3: Full Forward/Reverse S-Parameter Configuration



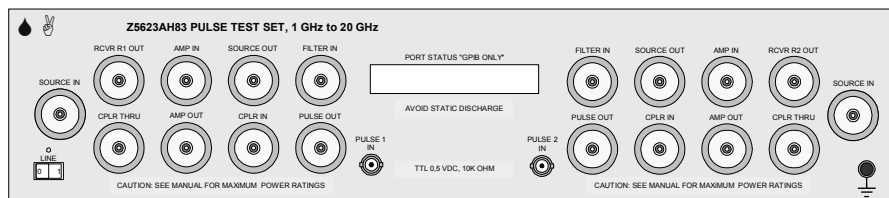
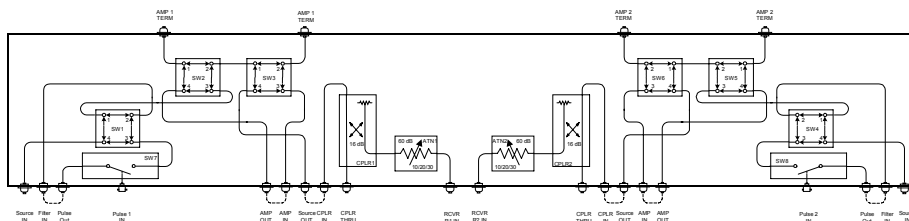
PNA Pulsed-RF Configuration Example 3: Full Forward/Reverse S-Parameter Configuration a different view



Z5623A H83 – H84 Test Set Control Macro

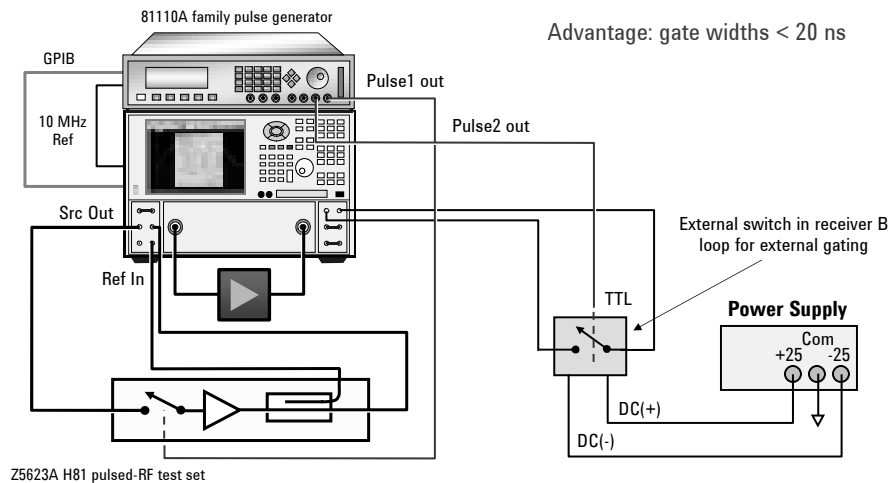


Z5623A H83 RF Modulator 1-20 GHz



PNA Pulsed-RF Configuration Example 4

- Modulator test set, external receiver gate
- Point-in-pulse, pulse profile



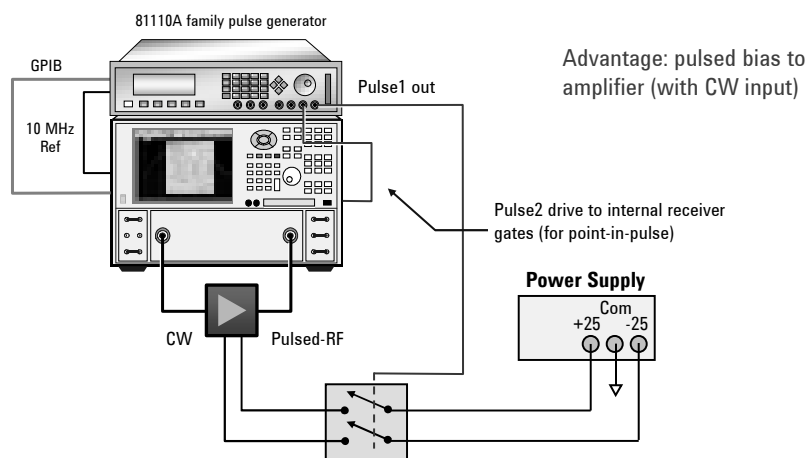
Page 37

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PNA Pulsed-RF Configuration Example 5

- User-supplied pulsed bias to amplifier, internal IF gate
- Point-in-pulse, pulse profile



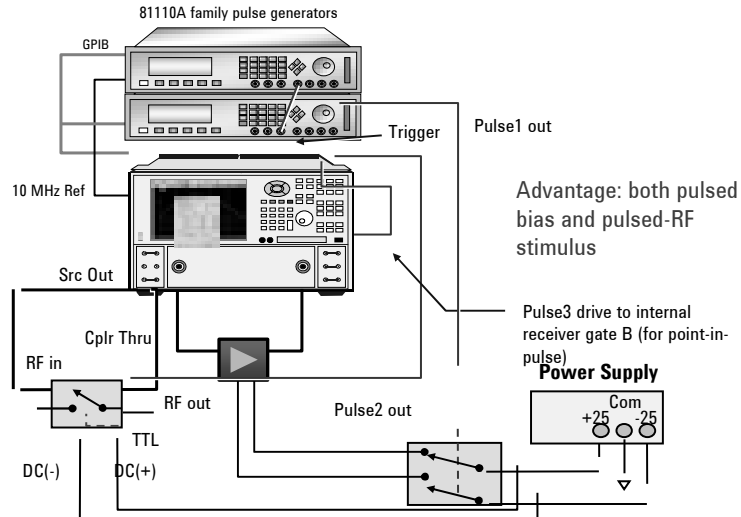
Page 38

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PNA Pulsed-RF Configuration Example 6

- Customer-supplied pulsed bias and pulsed RF, internal IF gate
- Point-in-pulse, pulse profile



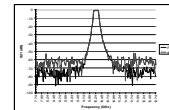
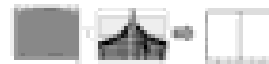
Page 39

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Summary

- Testing with pulsed-RF is very important for radar, EW, and wireless comms systems
- Narrowband detection:
 - Spectral nulling technique improves measurement speed
 - For radar and wireless comms applications, offers superior dynamic range/speed
 - No lower limit to pulse widths
- Although the PNA uses different hardware and detection techniques than the 8510, measurement results are essentially the same!
- PNA also offers numerous platform benefits:
 - Measurement flexibility (32 channels, 64 traces, 16 windows, 16,001 points)
 - Connectivity (LAN, USB, ...)
 - Automation (open Windows®, COM, SCPI ...)
 - Ease of use (built-in HELP, Cal Wizard, ECal ...)



Page 40

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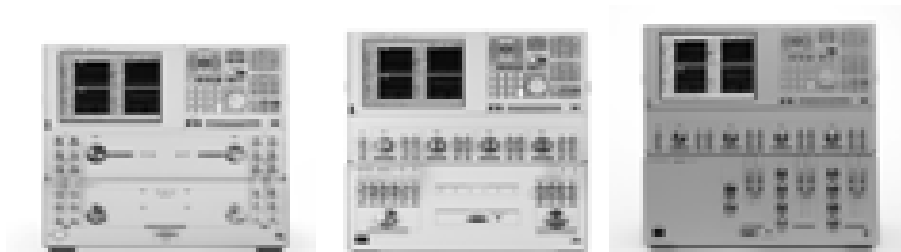
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Resources

- www.agilent.com/find/pulsedrf

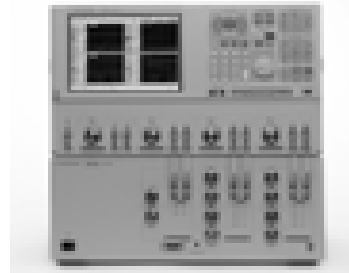


Multiport - PNA based solutions



Agenda

- **Target Applications** ←
- PNA Multiport Test Solutions
- Specials vs. Standard product
- Customer data required for new multiport specials
- Further Information

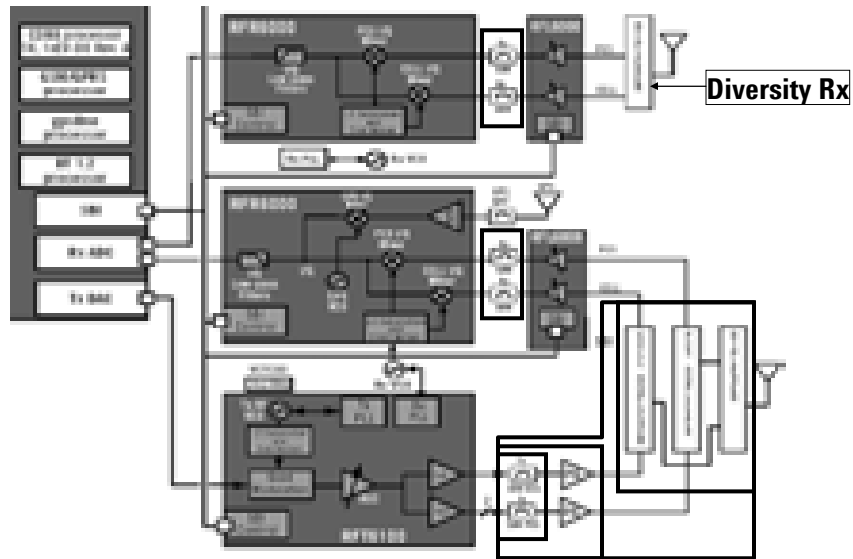


Target Applications

- Front End Module (FEM)
 - Cellular FEM (see next slide)
 - WLAN FEM (Base Band not included, 2.4G & 5G dual band)
 - Filter array (see next slide)
 - Multiple filter in single package
 - Duplexer/Coupler array (see next slide)
 - Multiple Duplexer/Coupler in single package
- High Frequency Multiport devices
 - Triplexer, power splitter, multiport coupler etc.
 - RF module, RF switch IC
- High power device testing

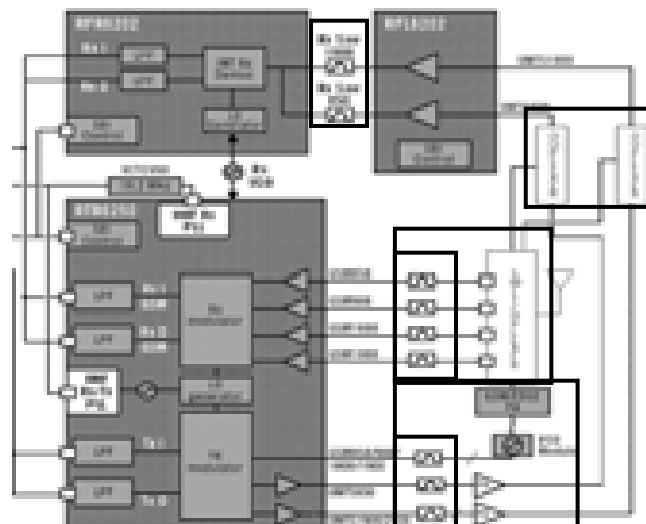


Cellular FEM #1 (Dual band, 1xEV, GPS)



Page 45

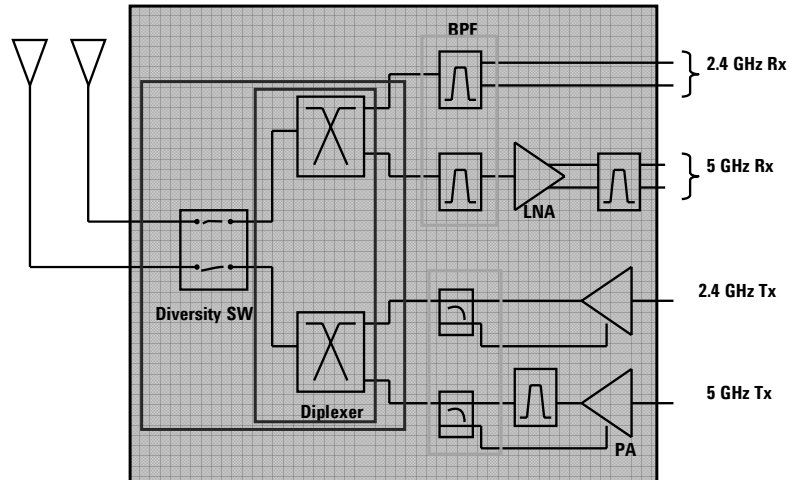
Cellular FEM #2 (Quad band, UMTS, GSM)



Page 46

WLAN FEM (2.4G•5G dual band)

2.4 GHz / 5 GHz WLAN FEM



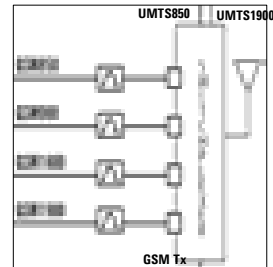
Multiport & High Power Testing Devices

- Typical High Frequency devices
 - Switches, Couplers, Power Splitter/Divider and etc..
 - Filter/Coupler array
- Multiport and high power
 - PA Cellular/WLAN FEM with PA
 - RF switch IC (Switch filters)

Key Measurement Requirements

Cellular FEM without PA

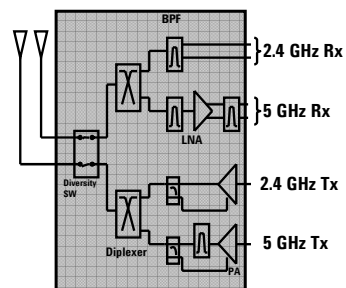
- IL, RL for each path up to 12.75GHz
- Isolation
 - Frequency > 3x Carrier
 - Signal level 0dBm or -10dBm
- Switch distortion
 - Frequency up to 12.75GHz in R&D
 - Signal Level up to +36dBm



Key Measurement Requirements

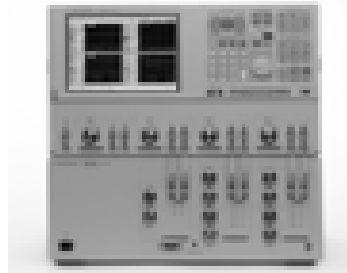
WLAN FEM with PA

- Gain, 1dB Compression, Pout, PAE
- RL
- Isolation
- Harmonics distortion
 - Frequency Cellular > 3x Carrier Frequency
 - Frequency (WLAN): 17.4GHz
 - Power : 25dBm(WLAN)
36dBm(GSM/Mobile)



Agenda

- Target Applications
- **PNA Multiport Test Solutions** ←
- Specials vs. Standard product
- Customer data required for new multiport specials
- Further Information



New PNA Rev 6.0 Firmware (Available December 2005)

Sets GP-IB address, or Test Set IO address

Select Testset Control File base on test set

New Functionality:

- External test set control
- “Any 2-port” capability

Set physical ports in ANY order

Set control lines (if test set has them) on a per channel basis

PNA/PNA-L Option 550

Measure

SParameter

Balanced

Receivers

Applications

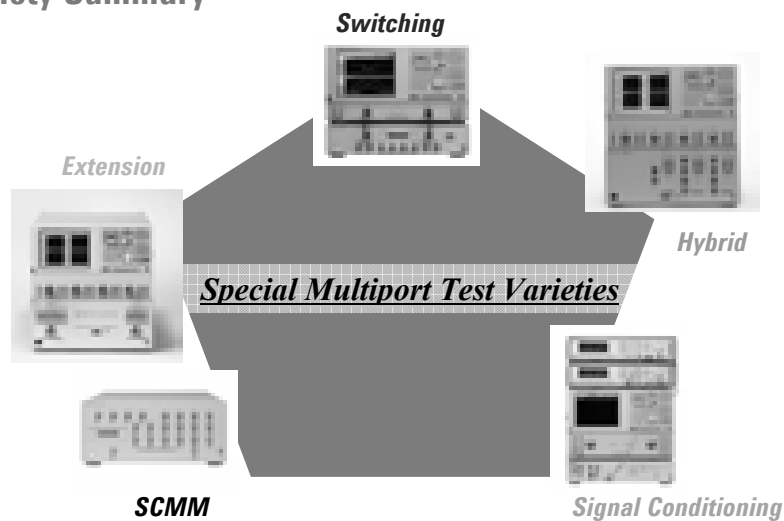
- New firmware option 550 for the PNA/PNA-L adds full 4-port capability and differential measurements to a two port network analyzer

- CPL Dec 1, 2005

- \$7k RFP



Variety Summary



Test Sets Overview		
<u>Platform</u>	<u>Description</u>	<u>Benefits</u>
87050A-Hxx/Kxx	Switching test sets. No coupler inside test set	Lower cost
N4419/20/21B/H67	Extension test sets Coupler on each port	4-port differential to 67Ghz
Z5623A-Hxx/Kxx	Depend on the particular option Mixing of Switching and Extension test sets	Meets customer specific req'ts

Agilent's Promoted Multiport Products & Specials

Model	Options	# of ports	Input BW	Input BW	Compatible MM's	Comments
81607B	414	4	300MHz	2.0GHz	-	analog isolation
81607B	414	4	300MHz	4.0GHz	-	analog isolation
81607B	414+42	4	300MHz	20GHz	-	analog isolation
81607B	-	4	10MHz	20GHz	SP's, PPA's, PPA's	Agilent's best all rounder for passive (pass, loss, re, gain)
81607B	-	4	10MHz	40GHz	SP's, PPA's, PPA's	Agilent's best
81607B	-	4	10MHz	50GHz	PPA's, PPA's	Agilent's best
81607B+P	-	4	10MHz	50GHz	PPA's	Agilent's 50GHz signal path isolation
81700B	814	4	3GHz	2.0GHz	SP's, PPA's	Agilent's best general matrix, good state switching
71607A	814	4B	300MHz	20GHz	PPA's/PPA's	passive and active, signal state out
81700C	814	4	3GHz	1.0GHz	SP's, PPA's	Matrix, full precision, full general matrix, cold state switches
81700C	814	4	3GHz	1.0GHz	SP's, PPA's	Matrix, full precision, full general matrix, cold state switches
81700C	814	4	3GHz	2.0GHz	SP's, PPA's	Matrix, full precision, full general matrix, cold state switches
81700C	814	4	3GHz	2.0GHz	SP's	Agilent's best general matrix, good state switching
71607A	814	4	1GHz	10GHz	PPA's	Agilent's best. Full general matrix, mechanical switch, fixed multiplex and RF switch for 1 GHz
71607A	814	4	1GHz	10GHz	PPA's	Agilent's best. Full general matrix, mechanical switch, cold state for port-to-port isolation and RF switch for 1 GHz
81607A	814	4	10MHz	20GHz	PPA's, PPA's	Agilent's best. Full general matrix, mechanical switch
81607A	814	4	50 MHz	50GHz	PPA's, Agilent PPA's	Agilent's best. Full general matrix, mechanical switch
81700C	814	12	3GHz	1.0GHz	SP's, PPA's	Matrix, full precision (12) general matrix, cold state switches
71607A	814	14	10MHz	20GHz	4 port PPA's	10 full loaded isolation test and other good with 4 full PPA's, Matrix
81600B	814	12	3GHz	2.0GHz	SP's, PPA's	Agilent's best 12 port general matrix, cold state switches
81700A	814	12	10MHz	20GHz	PPA's, PPA's	Agilent's general 12 port type, full matrix, mechanical switch, full precision, SP state switches available for 10GHz version
81607A	814	12	10MHz	20GHz	PPA's, PPA's	Agilent's 12 port general matrix, mechanical switch, cold state switches
81700A	814	24	10MHz	20GHz	PPA's, PPA's	Agilent's 24 port general matrix, mechanical switch

Specials



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Feb. 23, 2006

Page 56

Agilent PNA > 4-port Products offering

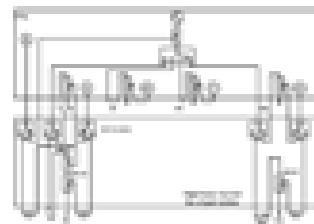
Freq.	Coverage:	PNA Based Unit & Ext. Test set	Total Test Ports
300 KHz – 20 GHz		N5230A opt. 245 & Z5623AK64	6
300 KHz – 20 GHz		N5230A opt. 245 & Z5623AK66	14
300 KHz – 20 GHz		N5230A opt. 245 & Z5623AKxx	20
.010 – 40GHz		E8363/4B or E8361A & 87050A-K62*	6

* 2-port cal only

Multiport Specials – Variety

• Extension Test Sets

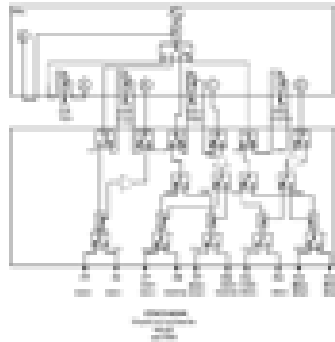
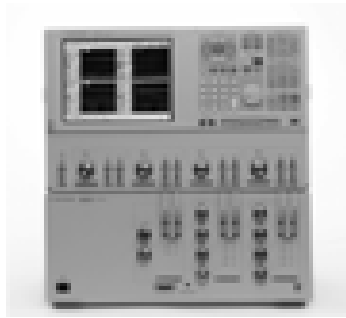
- Extension test sets provide signal paths from the network analyzer access ports to the test set. All test ports to the DUT are Coupler or Bridge base. Provides greater sensitivity.



Multiport Specials – Variety

• Hybrid Test Sets

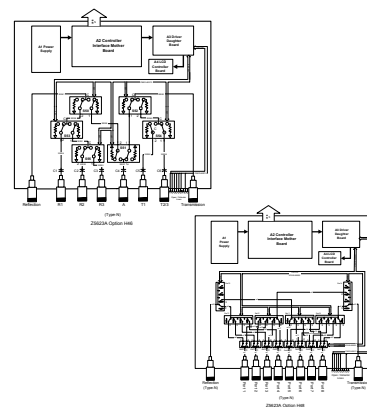
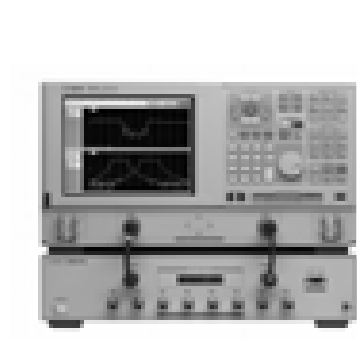
- Hybrid test sets are a combination of the switching and extension types. Test ports can be either switched or coupler bridge based.



Multiport Specials – Variety

• Switching Test Sets

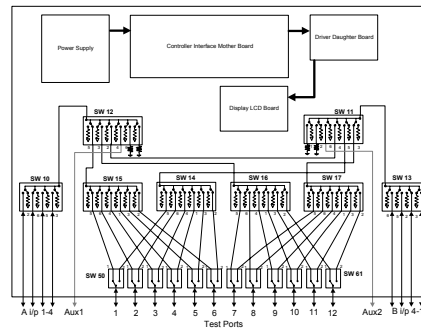
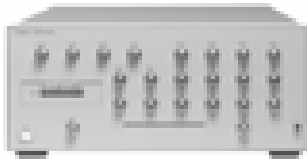
- Switching test sets provide signal paths from the network analyzer test ports to the DUT.



Multiport Specials – Variety

• SCMM

- Single connection multiple measurement test sets allow the user to make different types of measurements without having to disconnect their DUT from the test set.

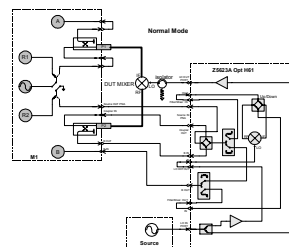
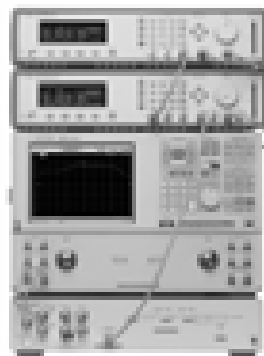


Agilent 8720D Option K22
Multi-Function Switch Matrix

Multiport Specials – Variety

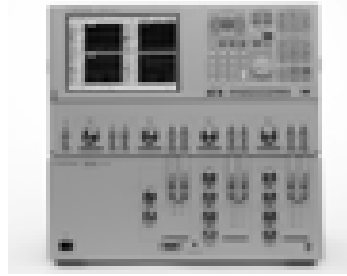
• Signal Conditioning

- Test sets that require couplers, attenuators, amplifiers, filters and mixers that may or may not directly connect to the DUT.



Agenda

- Target Applications
- PNA Multiport Test Solutions
- **Specials vs. Standard product** ←
- Customer data required for new multiport specials
- Further Information



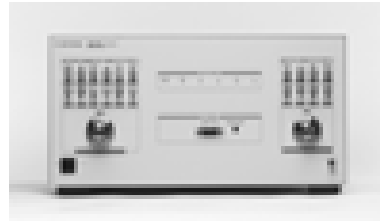
Multiport Specials – Why Specials?

- Offer solutions for applications which can not be addressed with existing or standard products
- Increase sales of CTD standard products
- Leverage standard platforms & OF capabilities to develop product extensions
- Fastest development-shipment time for new opportunities & competitive battles
- Helps to identify market needs and trends of specific applications

Multiport Specials –Specials vs. Standard product

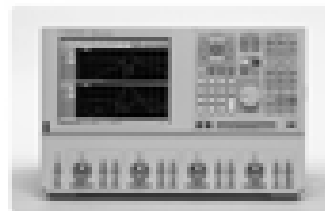
Multiport Special

- Custom
- Does not follow the NPI PLC process
- Fast development to shipment
- Typical supplemental performance
- Provide just enough performance
 - Functional Certificate
 - Return to Factory support



Standard Product

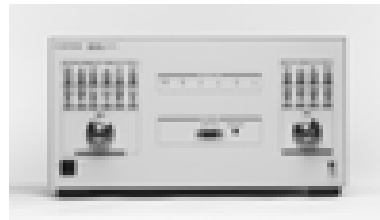
- Follows the NPI PLC process
- Specifications with uncertainties.
- Box and System level performance
- Calibration Certificate
- Return to Bench support
- Verification test



Multiport Specials –Test Set vs. System Performance

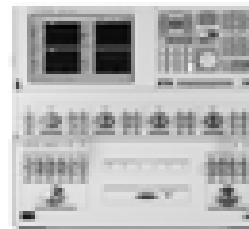
Multiport Test Set

- Typical supplemental performance specifications of the test set.
- Measures the Insertion Loss, Port Match, and path Isolation between ports.
- Provide just enough performance
- Functional Certificate



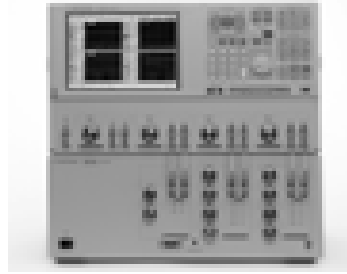
System Level (PNA and Test Set)

- Raw or Corrected system performance is not provided.
- Customers must take into consideration the performance of the PNA, Test Set, cabling, fixtures, and other peripherals to characterize their system level performance.
- Once established that system level performance meets the application requirements. The customer can now define the PNA Multiport Test Solution and calibrate the system.
- The customer can define a system verification method by using either a golden standard or by establishing an additional type of verification process.



Agenda

- Target Applications
- PNA Multiport Test Solutions
- Specials vs. Standard product
- **Customer data required for new multiport specials** ←
- Further Information



Multiport Qualification Form

- Most >4-port applications unique
- Define customer needs upfront
- Reduces time to quote and minimizes error

FE/AE fill out with customer and email back to CTD/Say Phommakesone

Qualification Form for Multiport Device

Device Description and Specifications

Describe the device and application (please attach block diagram of device)

Number of device ports: _____
 Port impedance: _____ 50 ohms _____ 75 ohms
 Connector type(s): _____ Type N _____ SMA _____ 3.5 mm _____ 2.4 mm _____ 1.85mm _____ other
 (if other, please explain) _____
 Specify the frequency range of the device: _____
 Specify the frequency range required for the device application: _____
 Specify required test port power: _____
 Specify Insertion loss / gain of the device paths: _____

Specify Isolation of other device ports: _____

Specify Port matches of the device: _____

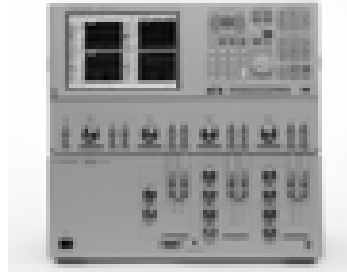
Specify desired measurement uncertainty: _____

Specify other measurement requirements: _____

If desired test system is complex (e.g. includes other analyzers, additional sources, etc), include block diagram of overall test setup.

Agenda

- Target Applications
- PNA Multiport Test Solutions
- Specials vs. Standard product
- Customer data required for new multiport specials
- **Further Information** ←



Information Sources

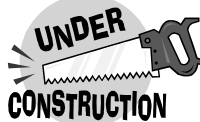
COST & ORDER		
Freq.	Coverage:	Ext. Test Set & #Ports
300 KHz – 20 GHz		Z5623AK64 2-port
300 KHz – 20 GHz		Z5623AK66 10-port
.45 – 20/40/50 GHz		N4419/20/21B 2-port
.45 – 67.0 GHz		N4421BH67 2-port

URLs

- <http://mktwww.soco.agilent.com/Product-Info/Network-Analyzers/PNA/multiport.htm>
- <http://www.agilent.com/find/multiport>
- <http://www.agilent.com/find/PNA>

JOB AIDS/SALES TOOLS

- Agilent Test Solution for Multiport and Balanced Devices 5988-2461EN
- Agilent PNA Series Configuration Guide 5988-7989EN



Summary

- PNA multiport test solutions provide:
 - Direct test set control made easy with PNA Firmware Rev 6.0s
 - Flexible test port configuration that enables customer to perform variety kinds of multiport device measurements
 - Advanced measurement capabilities, such as the APE, result in accurate measurements



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GigaTest Labs

Complete Characterization of Backplane Differential Channels

February 23, 2006

presented by:

Ming-Fan, Tsai
Agilent Technologies Ltd.

Overview

Backplanes
Measurement set up
Single-ended
Differential
Frequency & time domain
Eye diagrams
Model extraction

All Next Generation High Speed Serial Links will use Differential Signaling

Serial ATA	1.25 Gbps
Hypertransport	1.6 Gbps
AGP8x	2.1 Gbps
Infiniband	2.5 Gbps
PCI Express	2.5 Gbps
Serial ATA II	2.5 Gbps
XAUI	3.125 Gbps
PCI Express II	5.0 Gbps
OC-192	9.953 Gbps
10 GbE	10 Gbps
OC-768	39.81 Gbps

Important Physical Layer Properties of Differential Channels

Differential impedance profile (diff return loss)

Transmitted differential signal quality (diff insertion loss)

Conversion of differential to common signal

Where conversion of differential to common signal occurs

Eye diagrams (1 Gbps → 10 Gbps)

Measurement System for Complete Physical Layer Characterization



Differential VNA/TDR Applied to All Passive, Linear Components and Interconnects

- When an external precision signal is required
- Applies to any passive interconnect or component
 - Backplanes
 - Discretes
 - Packages
 - Connectors
 - PCB structures
 - Material properties



Page 77

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A Precision Instrument is Not Enough!

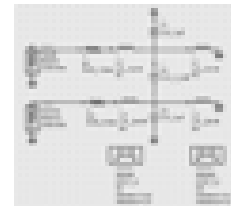
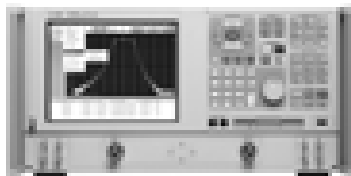
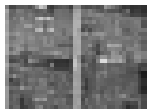
Component to
characterize

-?→

Instrument

-?→

Valuable
information

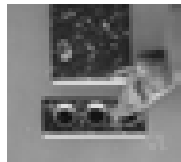


Page 78

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Complete Characterization System Solution



**DUT +
microprobes**

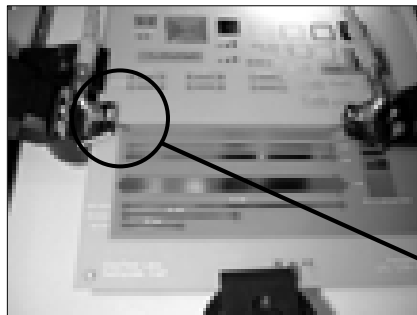


**GigaTest Probe
Station**

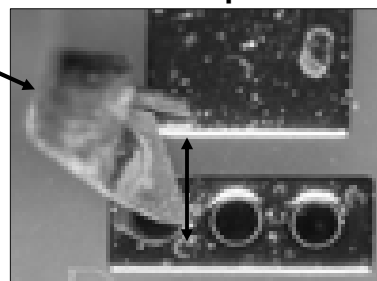


**Physical Layer Test System:
VNA + PLTS software**

Microprobes Allow Precision Probing of Structures with Minimal Artifacts

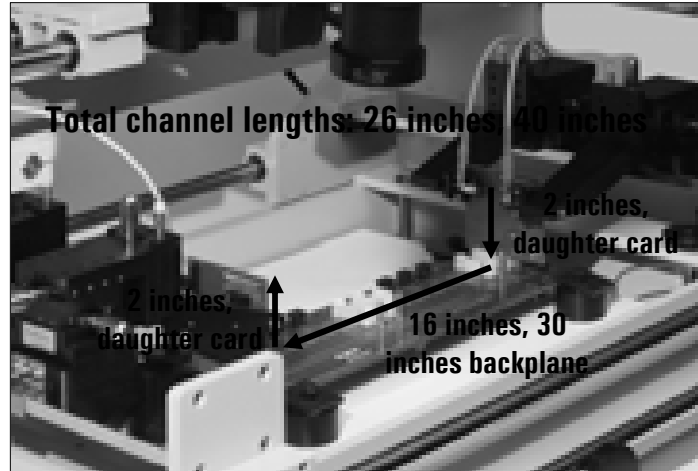


Close up



Pitch ~ 50 μ – 1000 μ

4 Port Differential VNA Techniques Applied to Tyco Electronics HM-Zd Legacy Backplane System

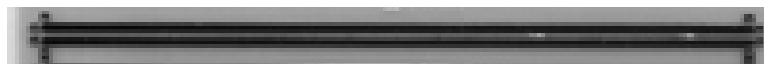


Page 81

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4 Port Single-ended S-parameters



1 2
3 4
(and their return paths!)

$$S_{out,in} = \frac{P_{out}}{P_{in}}$$

Stimulus

Response	S_{11}	S_{12}	S_{13}	S_{14}
	S_{21}	S_{22}	S_{23}	S_{24}
	S_{31}	S_{32}	S_{33}	S_{34}
	S_{41}	S_{42}	S_{43}	S_{44}

Interpreting single ended measurements:

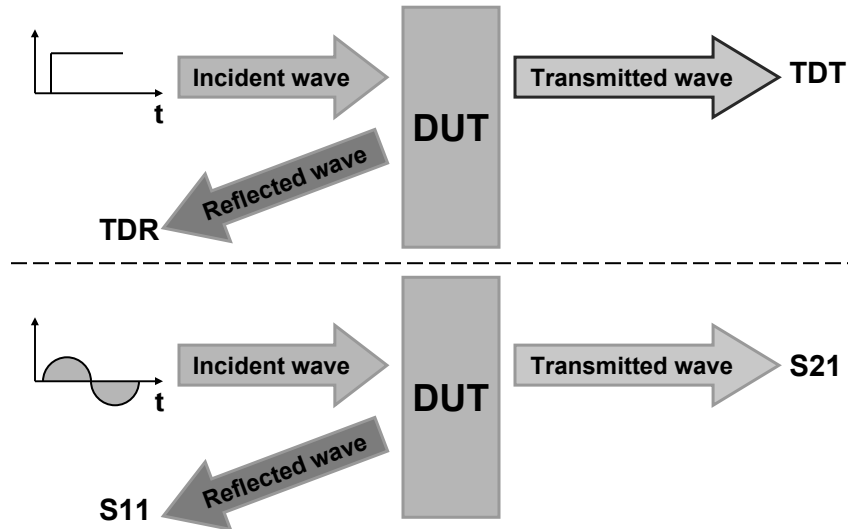
S_{11} : return loss, single ended
 $S_{21} = S_{12}$: insertion loss, single ended
 $S_{31} = S_{13}$: near end cross talk
 $S_{41} = S_{14}$: far end cross talk

Page 82

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TDR and VNA Techniques

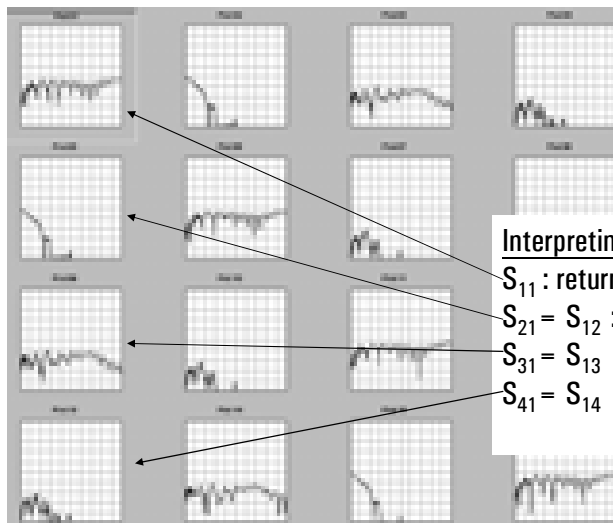


Page 83

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4 Port, Single-ended S-parameters: Tyco Backplane Example



Interpreting single ended measurements:

S_{11} : return loss, single ended

$S_{21} = S_{12}$: insertion loss, single ended

$S_{31} = S_{13}$: near end cross talk

$S_{41} = S_{14}$: far end cross talk

Page 84

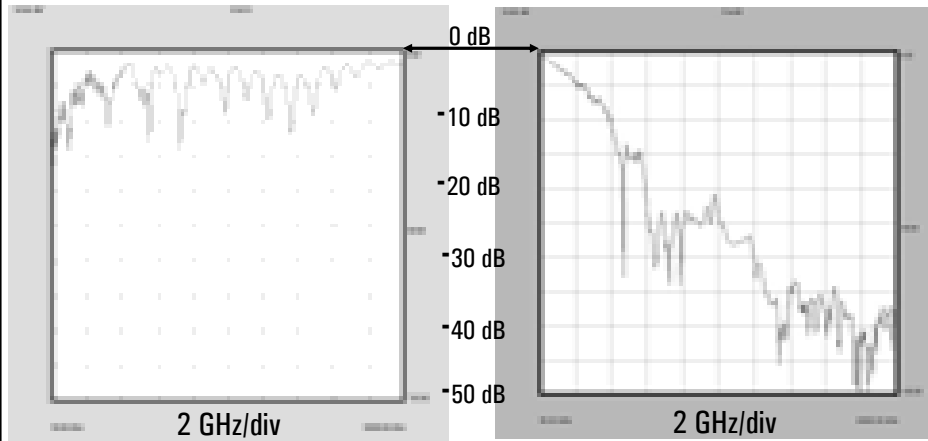
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Single-ended Return Loss and Insertion Loss: 26 inch channel length

Input Single-ended Return Loss S11

Input Single-ended Insertion Loss S21

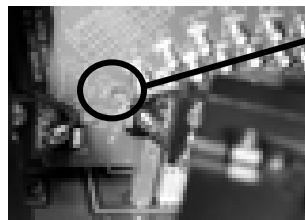
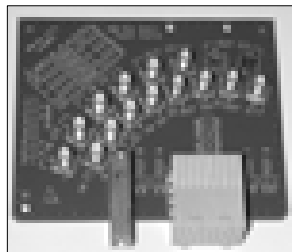


Page 85

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Microprobing on SMA Pads



Added ground pad

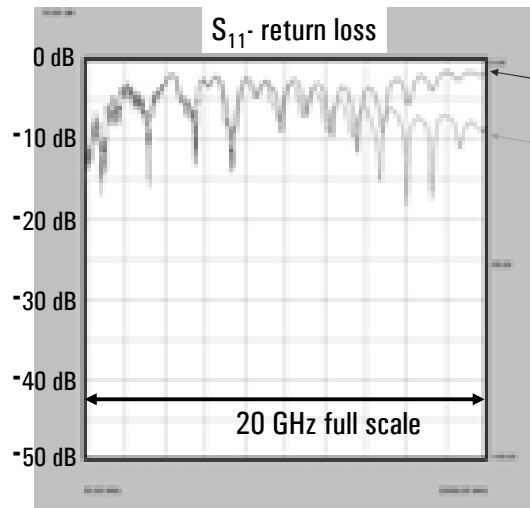


Page 86

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Bandwidth Limit of SMA vs. Microprobes



Measured with SMA connector

Measured with microprobe

Conclusions:

1. Microprobes can be higher bandwidth (important > 14 GHz)
2. Identical performance < 10 GHz for these SMA connectors

Page 87

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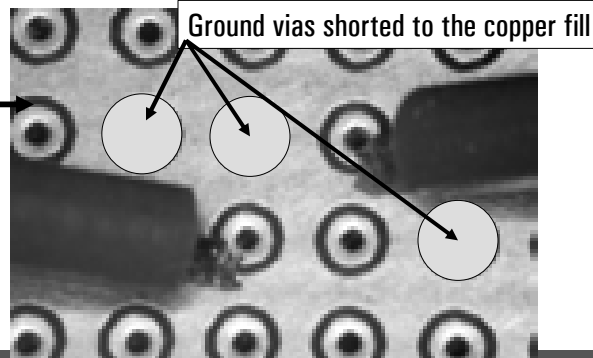
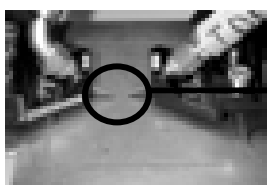
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Design for Test (DFT): Optimized Pad Design for Micro-probing

Any signal via can be used as a probe point

Use a "copper fill" around the signal via with immediate connection to all adjacent ground vias

Every board should be designed with pads for optional microprobing- no impact on function



Page 88

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Microprobing vs. SMA Connectors

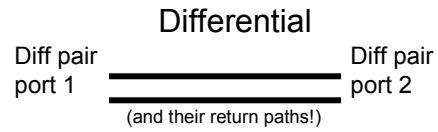
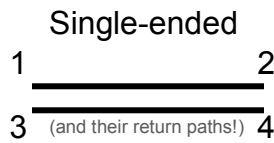
	Strengths	Weaknesses
SMA Connectors	• No additional fixturing to VNA required • Easy to use • Mechanically robust	• Can't use on functional boards- loads the line too much • Limited density
Micro Probes	• Can use on any signal lines • No constraints on how many or where • Can be used on functional board • Important for active probing	• Probe station required • Probes can be damaged

Two Important Transformations Facilitate First Order Analysis

From single-ended S-parameters to differential S-parameters

From frequency domain to time domain

4 Port Balanced Measurements: Frequency and Time Domain



Stimulus

Response	S_{11}	S_{12}	S_{13}	S_{14}
	S_{21}	S_{22}	S_{23}	S_{24}
	S_{31}	S_{32}	S_{33}	S_{34}
	S_{41}	S_{42}	S_{43}	S_{44}

Stimulus

Response	Differential Signal		Common Signal	
	Port 1	Port 2	Port 1	Port 2
Differential Signal	S_{DD11}	S_{DD12}	S_{DC11}	S_{DC12}
Port 1	S_{DD21}	S_{DD22}	S_{DC21}	S_{DC22}
Port 2	S_{CD11}	S_{CD12}	S_{CC11}	S_{CC12}
Common Signal	S_{CD21}	S_{CD22}	S_{CC21}	S_{CC22}
Port 1				
Port 2				

The Meaning of the Quadrants

Differential in, differential out:
Behavior of differential signals

Common in, differential out:
Behavior of mode conversion

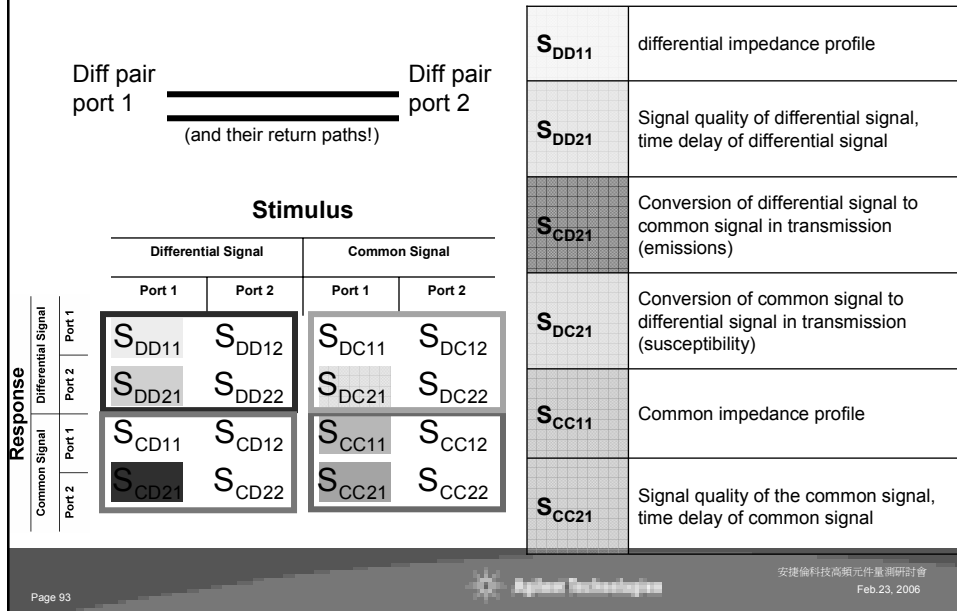
Stimulus

Response	Differential Signal		Common Signal	
	Port 1	Port 2	Port 1	Port 2
Differential Signal	S_{DD11}	S_{DD12}	S_{DC11}	S_{DC12}
Port 1	S_{DD21}	S_{DD22}	S_{DC21}	S_{DC22}
Port 2	S_{CD11}	S_{CD12}	S_{CC11}	S_{CC12}
Common Signal	S_{CD21}	S_{CD22}	S_{CC21}	S_{CC22}
Port 1				
Port 2				

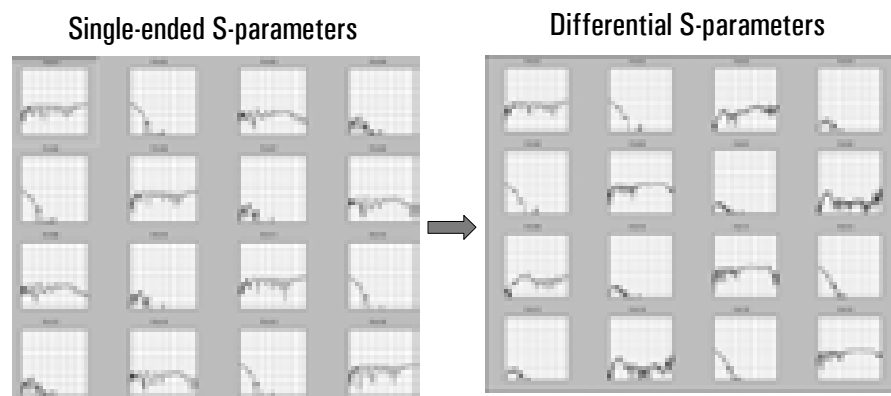
Differential in, common out:
Behavior of mode conversion

Common in, common out:
Behavior of common signals

Important Performance Terms

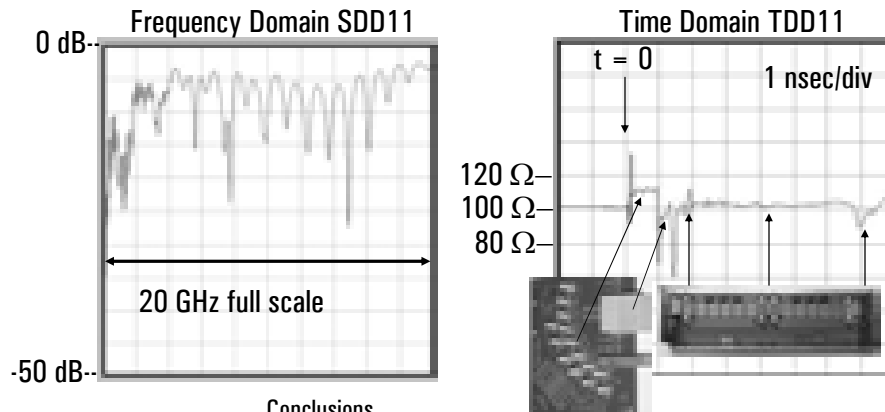


Single-ended to Differential S-parameters



Note: One measurement with Physical Layer Test System yields above information

Differential Return Loss & Reflection Coefficient



Conclusions

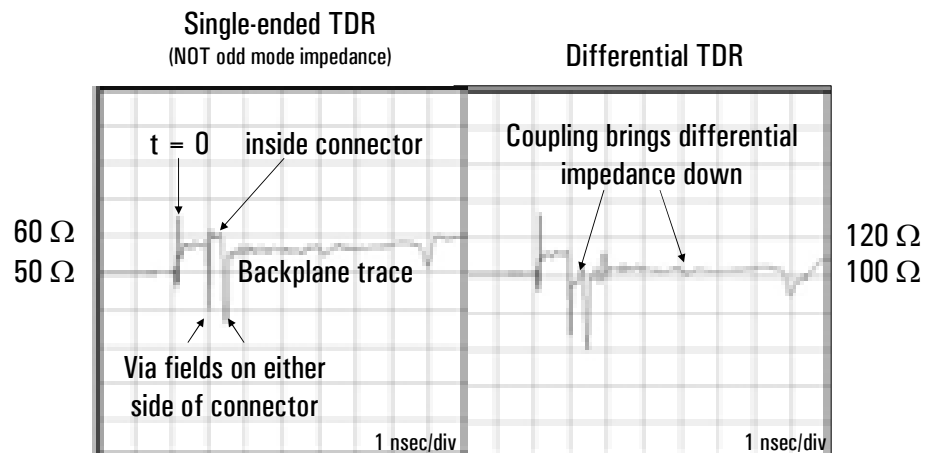
- Connectors create large impedance discontinuity
- Daughter card differential impedance is 110 Ω
- Backplane differential impedance is 102 Ω

Page 95

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Single-ended and Differential TDR



Page 96

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Important Design Feedback

Designing for 50 Ohm single ended line is not the same as a 100 Ohm differential line.

Characterizing with single ended TDR will not measure differential impedance.

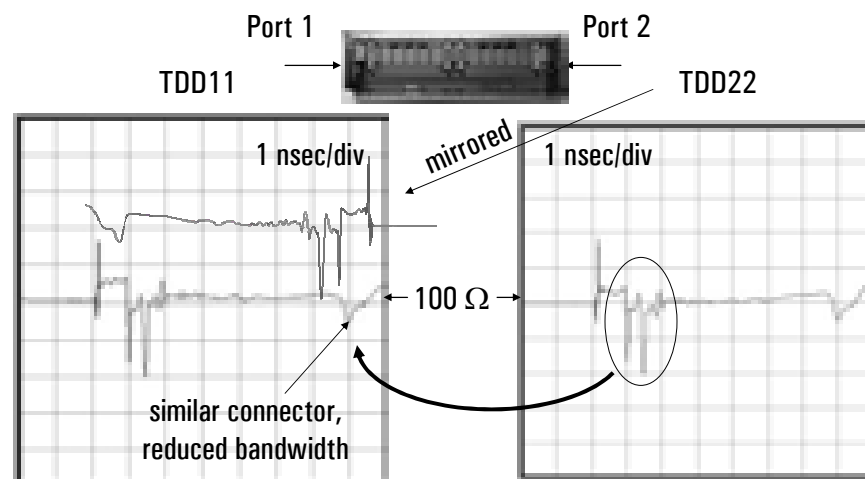
Design the daughter cards with as much care as the backplane.

Most discontinuities from connectors are not from the connectors- they are from the via fields.

Optimizing connectors is all about optimizing the circuit board via field layout.

Design for test: add copper fills for microprobing

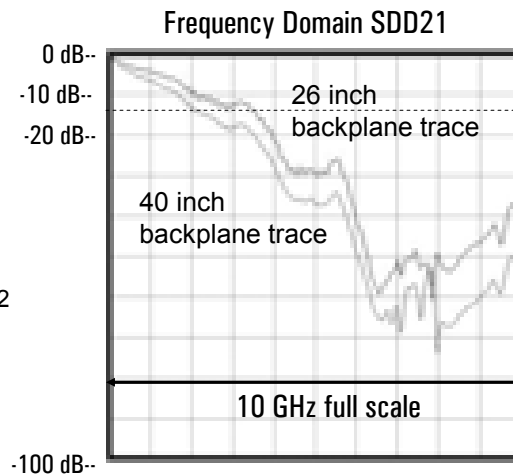
Differential TDR from Both Ends



Differential Transmitted Signal SDD21

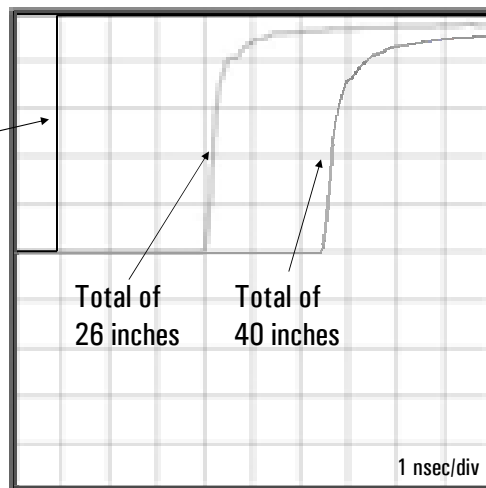
Conclusions:

- Measurement system bandwidth > 40 GHz
- 26 inch traces have a 15 dB BW ~ 3.5 GHz
- 40 inch traces have a 15 dB BW ~ 2 GHz

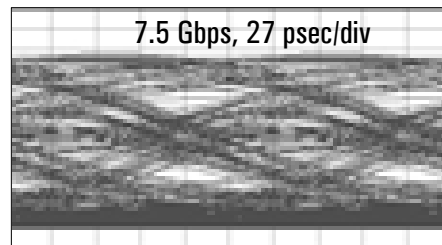
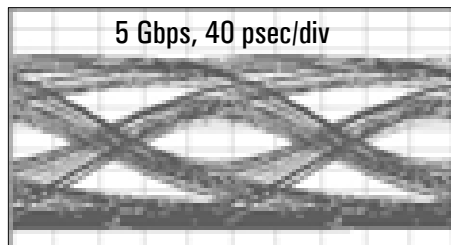
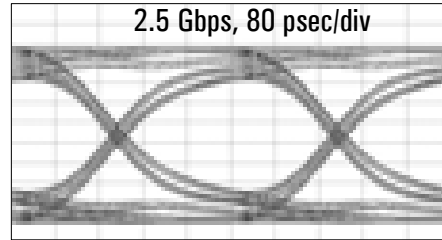
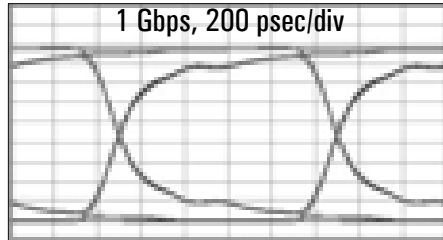


Differential Transmitted Signal: Time Domain TDD21

40 GHz bandwidth,
~ 20 psec input rise
time



Eye Diagrams: 26 inch Channel



Non-ideal Differential Signaling: Mode Conversion

Anything that affects one line and not the other will convert differential signal into common signal

Drive is asymmetrical between channels

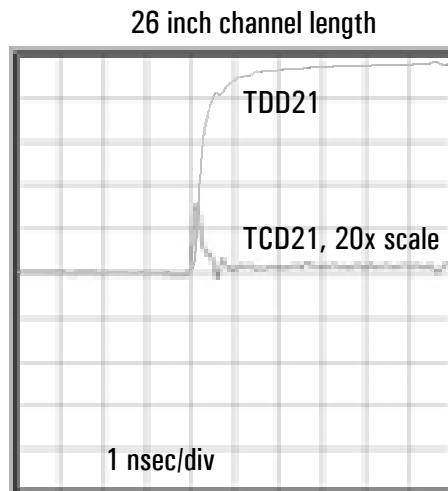
- skew
- output impedance and launched voltage

Signal environment in interconnect is asymmetrical

- different characteristic impedance in each leg
- length is different
- loading from connectors, jags, pads, ground planes

Real problem of common signal is EMI from unshielded twisted pair

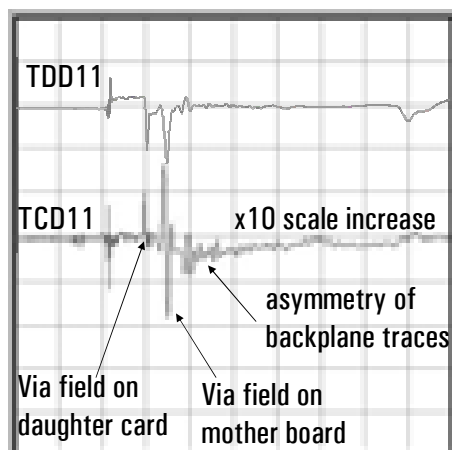
Differential Signal Input → Common Signal Output



~ 7% of differential signal amplitude converted to common signal

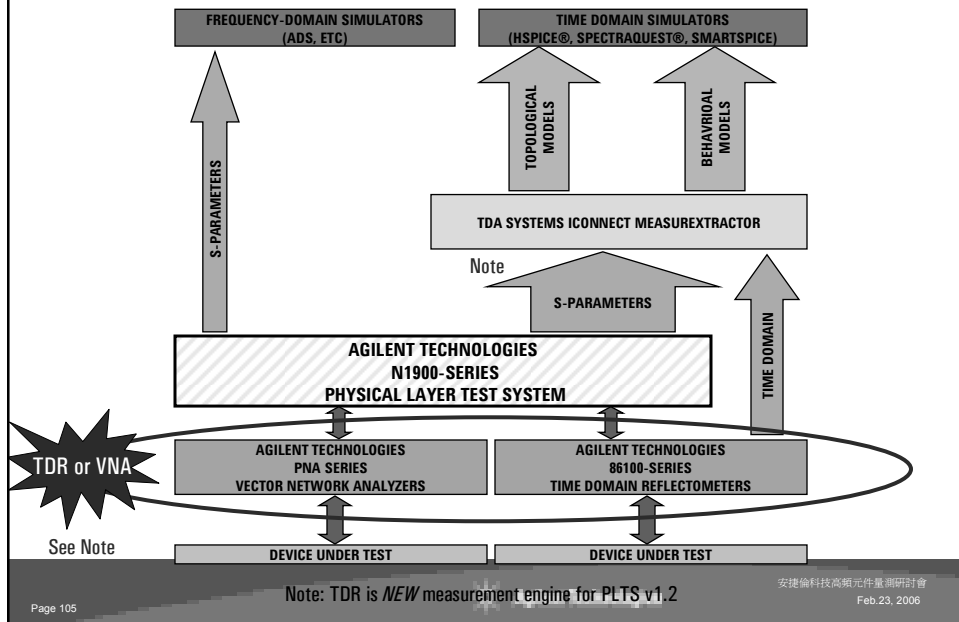
May be a problem if it were on CAT5 twisted pair

Where did the Conversion Happen?

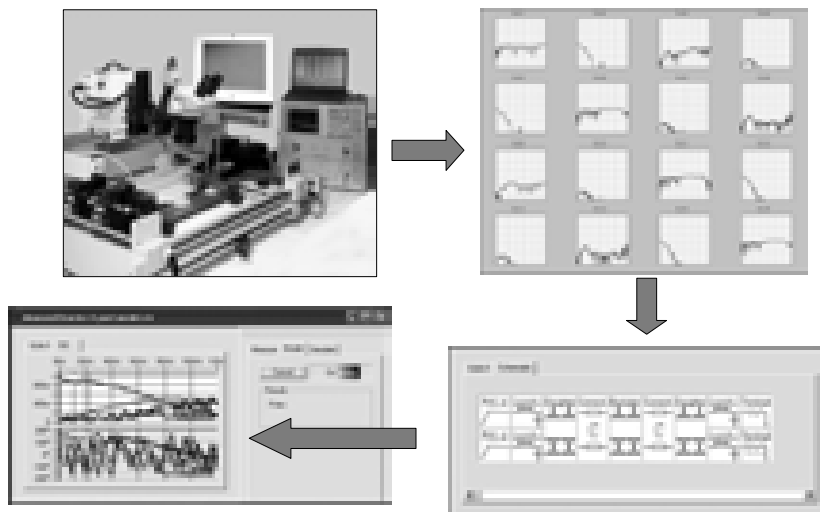


Conclusion: most mode conversion happens in the via fields!

Measurement and Model Extraction



Modeling Example with PLTS & IConnect



Conclusions

Differential pairs will proliferate

Differential characterization requires

- microprobes
- probe station
- 4 port VNA
- Analysis software

Absolutely everything you ever wanted to know about the performance of a differential pair is contained in the 4 port balanced S parameters- displayed in either the frequency or time domain

Technical Information Resources

Visit www.gigatest.com for..

- More than 100 application notes on high speed design
- Schedule of signal integrity short courses
- High-bandwidth measurement and modeling services
- Complete signal integrity characterization systems

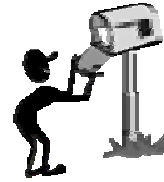
- Visit www.agilent.com/find/plts for..
 - Physical Layer Test System data sheet & user's guide
 - Signal integrity solutions brochure
 - XAUI backplane design case study
 - PCI Express tools brochure
 - N1900 series product flyer

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Enhanced TDR Channel Characterization Capabilities

Agilent Technologies Ltd.

Brian Chi
Senior Project Manager
Agilent Technologies
brian-tn_chi@agilent.com
03-4959054

Feb, 23, 2006

Page 1



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Impedance in Time Domain



High Speed Digital Design

Page 2

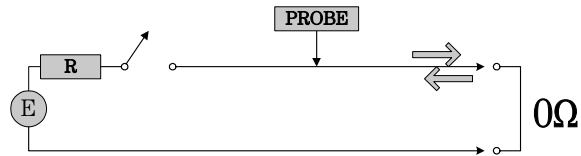


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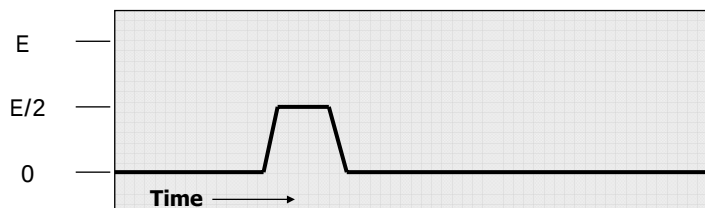
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Impedance in Time Domain

Short Termination

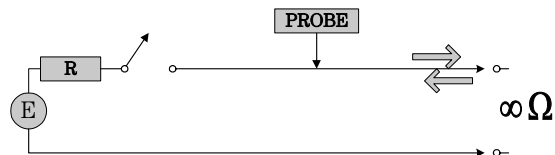


What do you expect to see at the probe before, during, and after you close the switch?

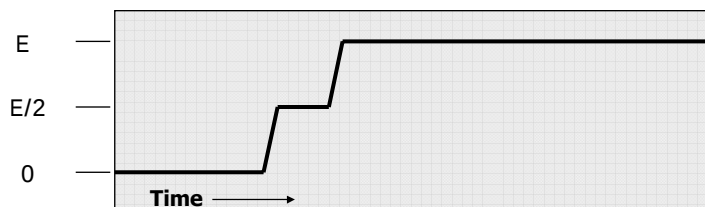


Impedance in Time Domain

Open Termination

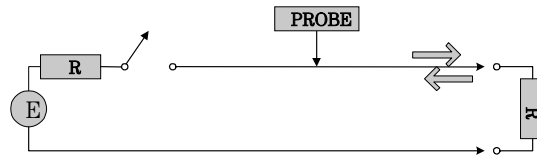


What do you expect to see at the probe before, during, and after you close the switch?

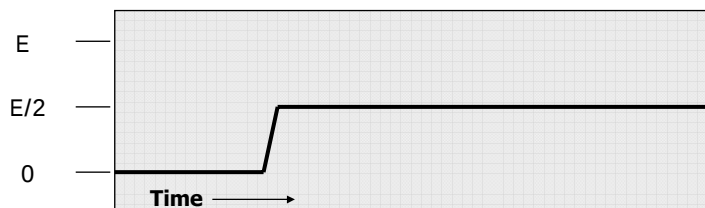


Impedance in Time Domain

Perfect Termination



What do you expect to see at the probe before, during, and after you close the switch?



Impedance in Time Domain

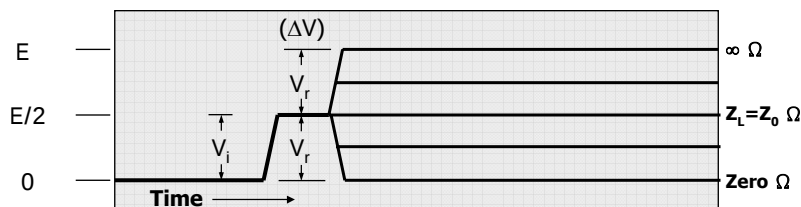
Impedance Mismatch Terms

$$Z_L = Z_0 \frac{1 + \rho}{1 - \rho}$$

Impedance Calculated from
Source Impedance and
Reflection Coefficient.

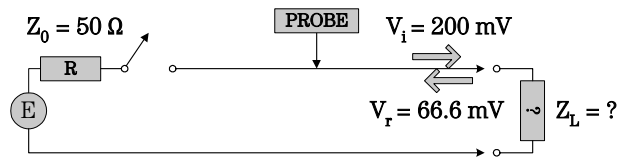
$$\rho = \frac{V_r}{V_i}$$

Reflection Coefficient:
How much was reflected?

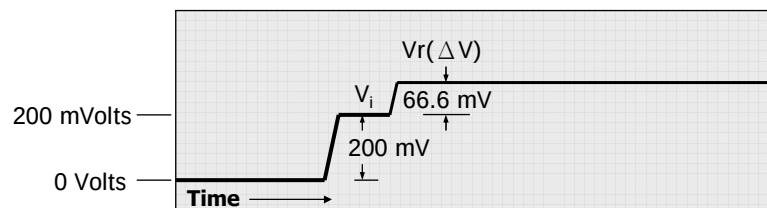


Impedance in Time Domain

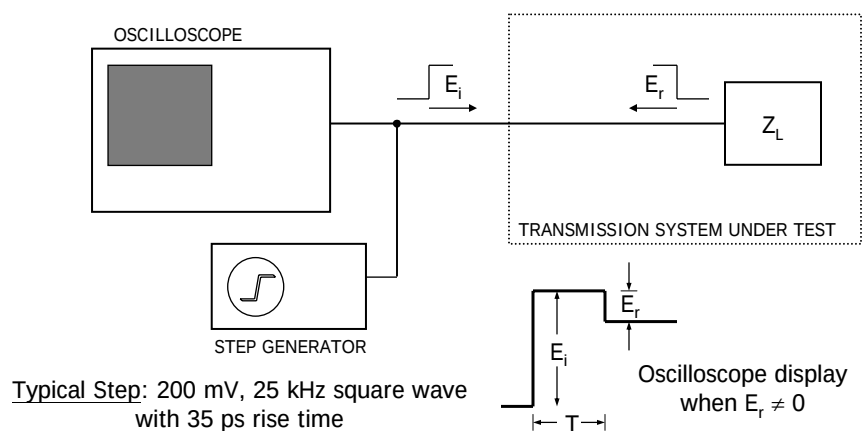
Mismatch Exercise



What is the value of Z_L ?



Step Reflection Testing



Mismatches Location

Distance Formula

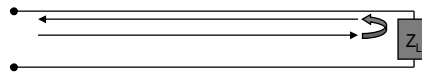
Where

V_p = velocity of propagation

T = transit time from monitoring point to the mismatch and back

$$D = v_p \cdot \frac{T}{2}$$

Why is the transit time divided by two?

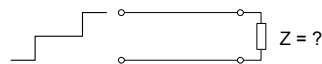


Simple Loads Reflection Analyzing

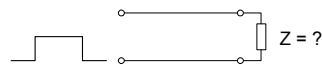
The shape of the reflected wave reveals the nature and magnitude of the mismatch

What is the nature of each of the loads shown at the right?

- a) SHORT
- b) OPEN
- c) IMPEDANCE $> Z_0$
- d) IMPEDANCE $< Z_0$



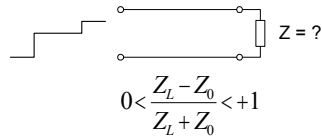
$$\frac{Z_L - Z_0}{Z_L + Z_0} = +1$$



$$\frac{Z_L - Z_0}{Z_L + Z_0} = -1$$

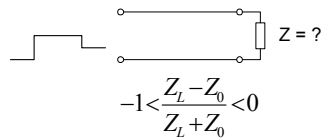
Simple Loads Reflection Analyzing

The shape of the reflected wave reveals the nature and magnitude of the mismatch



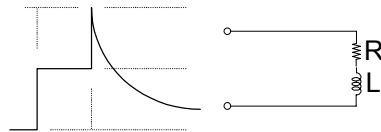
What is the nature of each of the loads shown at the right?

- a) SHORT
- b) OPEN
- c) IMPEDANCE $> Z_0$
- d) IMPEDANCE $< Z_0$



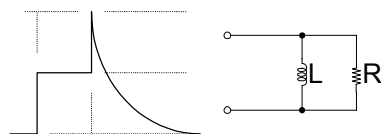
Complex Loads Reflection Analyzing

The shape of the reflected wave reveals the nature and magnitude of the reflection



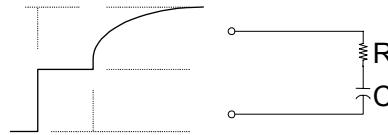
Complex load impedances are also identified

- Series R-L
- Shunt R-L



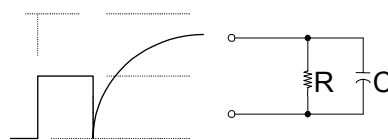
Complex Loads Reflection Analyzing

The shape of the reflected wave reveals the nature and magnitude of the reflection

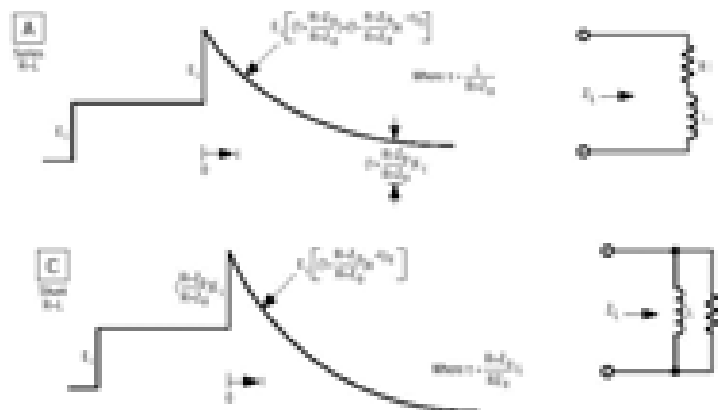


Complex load impedances are also identified

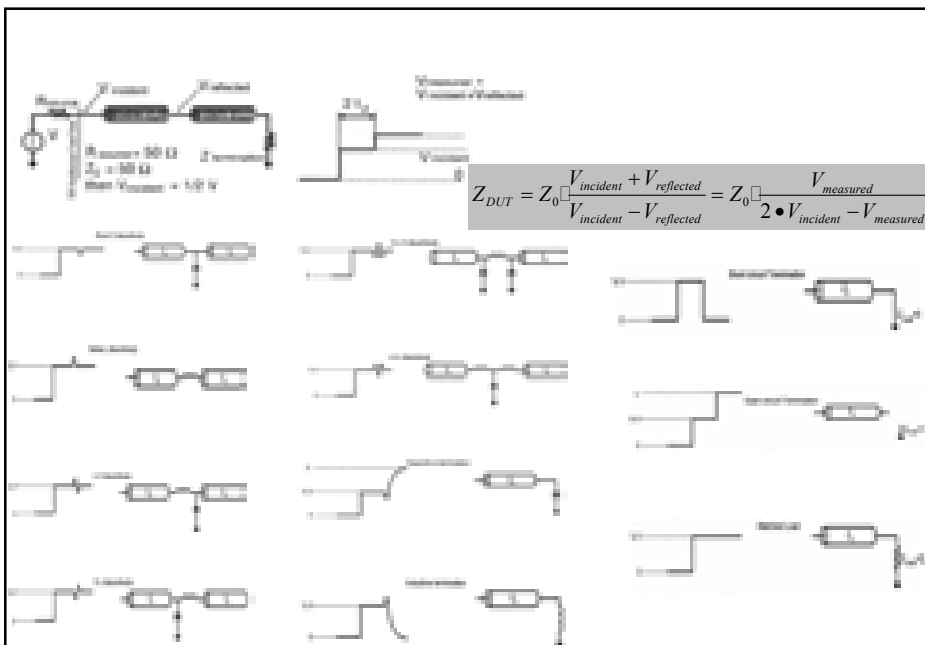
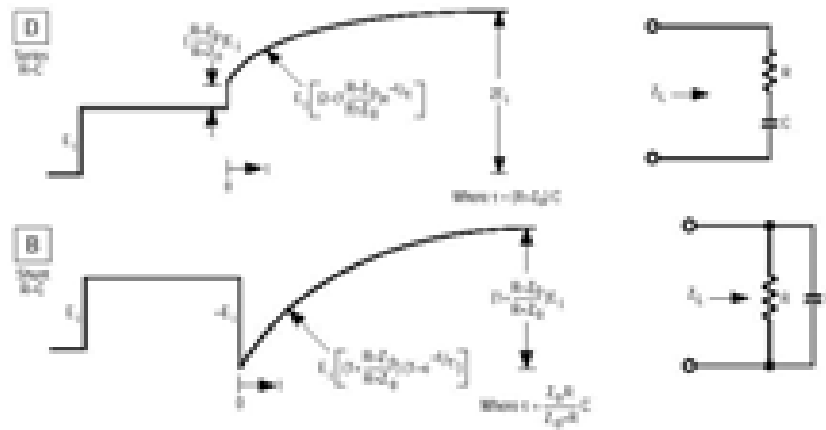
Series R-C
Shunt R-C



Analyzing Reflections of Complex Loads



Analyzing Reflections of Complex Loads



Required Parameters by Standard – S

Standard	Max Freq, GHz	Impedance	Return Loss S11	Loss S21	Crosstalk
PCI Express Gen 2	5	X	X	X	
PCI Express	1.25	X	X	X	X
PCI-X		X			X
Serial Attached SCSI	7.5	X			
IPC	N/A	X			
Fully Buffered DIMM	2.4		X		
IEEE 802.3ae	?	X	X		
Infiniband	6.3	X		X	X
Serial ATA	4.5	X		X	X
EIA-364-90	N/A	X			X
EIA-108	N/A	X	X		
HDMI	4.1	X		X	X
DVI	4.1	X			
Firewire	8	X		X	X
USB 2.0	1.3	X		X	
RapidIO	8				

Add: FSB, 1 GbE

IPC was Institute of Interconnecting and Packaging Electronic Circuits

Page 17



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Introducing 86100C option 202 - TDR S-Parameters capability

S-parameter display

TDR -> S11 (Return loss)

TDT -> S21 (Insertion loss)

Single-end & Differential

No external PC needed

Run on only 86100"C"



Page 18



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Introducing 86100C option 202 - Corrected Impedance Profile - Peeling

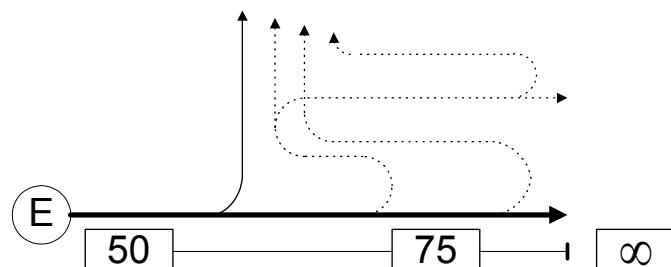
Peeling mitigate measurement errors caused by multiple reflections at each impedance mismatch.



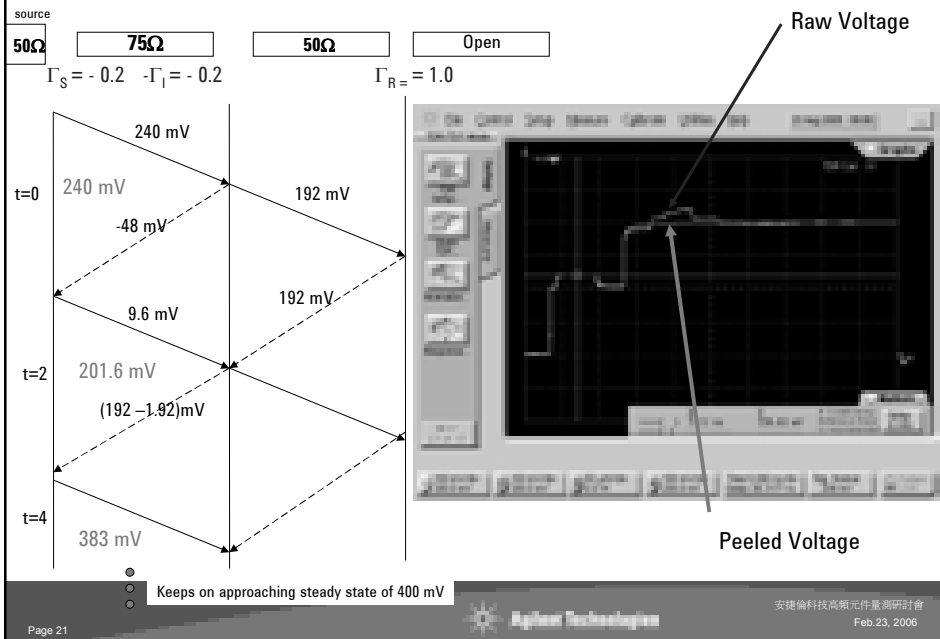
Blue: raw data
Yellow : corrected

Matching source Z_0 to transmission line Z_L

WHAT IF THE TRANSMISSION LINE OR CABLE
DOES NOT MATCH THE SOURCE IMPEDANCE?
WHAT WILL THE RESPONSE LOOK LIKE?



Peeling - Voltage Bounce Diagram



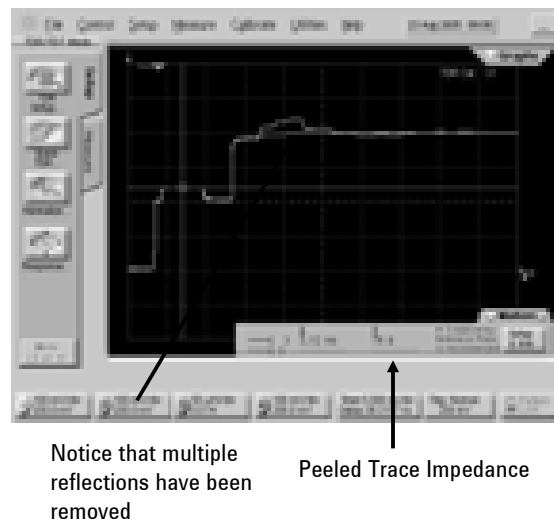
Corrected Z Profile into a 75 Ω Cable

Peeling assumes
Loss-less device.

Loss, Resistance [R],
degrade accuracy of
peeling.

Initial Z mismatch is
the most accurate.

Benefit is enhanced
with TDR calibration



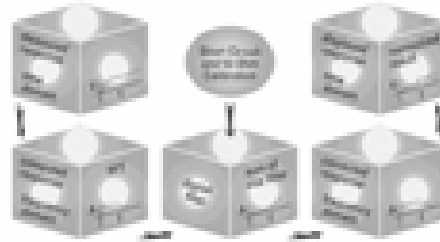
TDR normalization (As VNA's Calibration)

What is Normalization?

- Built-in Firmware
- Removes Test Fixture Error
- Increases Accuracy
- Allows Customer to Simulate his own system risetime

Originally Licensed from Stanford University (Bracewell Transform)

Critical for Rambus!



The procedure of TDR Normalization

- First part of the calibration removes systematic errors due to trigger coupling, channel crosstalk, and reflections from cables and connectors by measuring the response with the DUT replaced by a short circuit.
- The second part of the calibration generates a digital filter. The filter removes errors by attenuating or amplifying and phase-shifting components of the frequency response as necessary.
- For TDR, this is done by replacing the DUT with a termination having an impedance equal to the characteristic impedance of the transmission line, all of the energy that reaches it will be absorbed.

The procedure of TDR Normalization

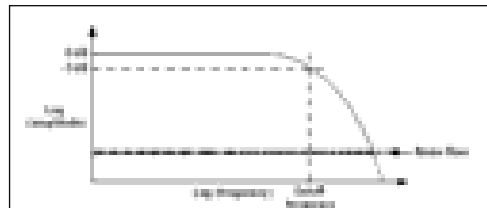


Figure 12. Basic system frequency response.

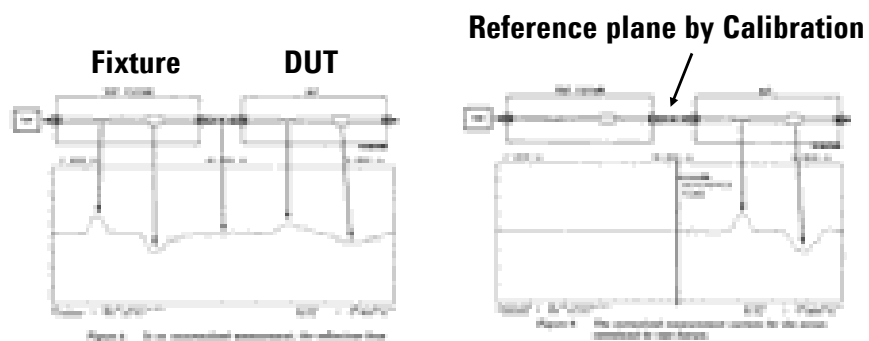


Figure 13. Normalized system frequency response (system bandwidth reduced).



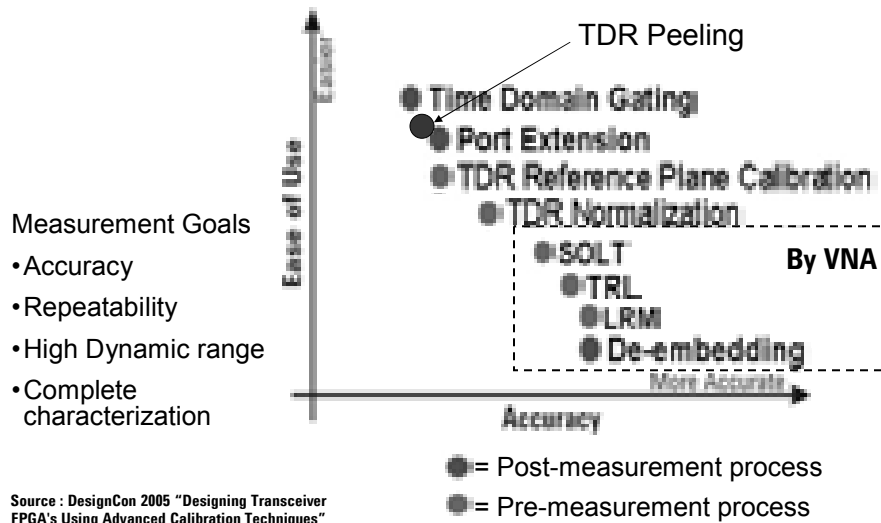
Figure 14. Normalized system frequency response (system bandwidth increased).

Effect of TDR Normalization Calibration



Remove Error caused by Test Fixture, Cable, connectors

Fixture Error Correction Techniques



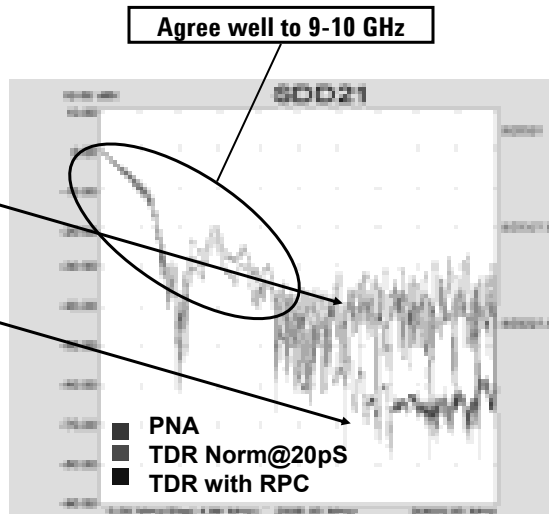
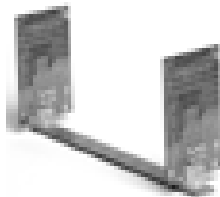
Page 27

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Comparison of TDR and PNA

- TDR has wide band receiver
 - Higher noise floor
 - Lower S/N ratio
 - Lower dynamic range
- VNA has narrow band receiver
 - Lower noise floor
 - Higher S/N ratio
 - Higher dynamic range

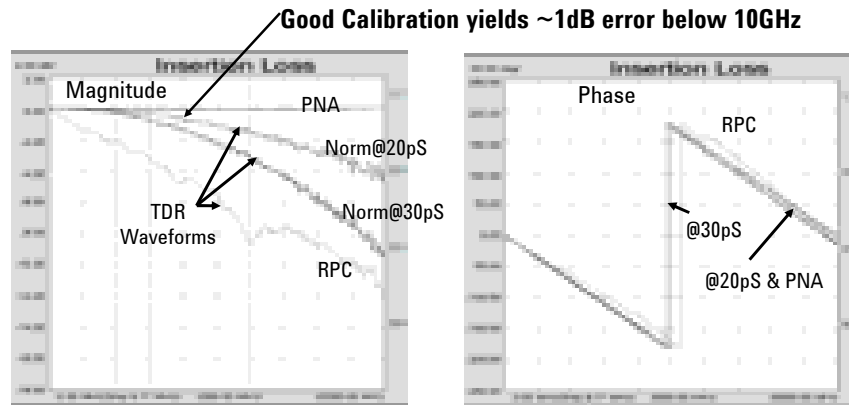


Page 28

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Comparison of TDR and PNA (Error Correction)



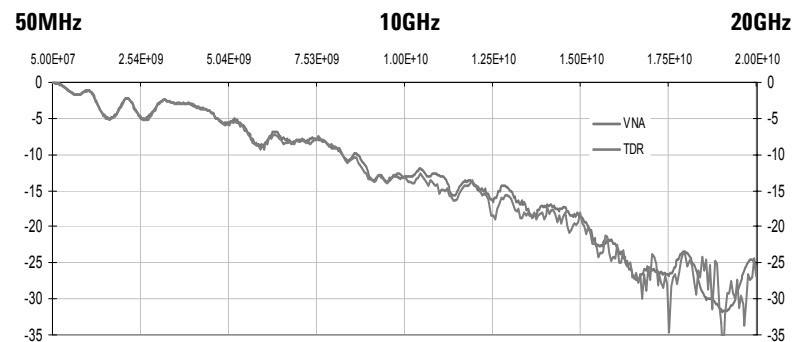
Comparison: TDR Calibration Methods versus PNA SOLT Calibration

Device Under Test: 3.5 mm Thru Adapter

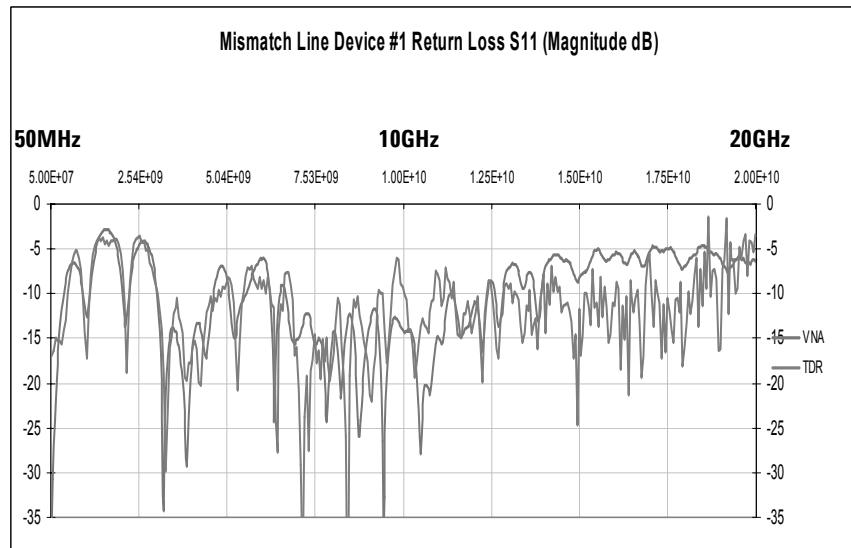
Results: The magnitude loss increases as a function of frequency and is dependent up calibration method for TDR-based measurements. Phase error due to timing jitter exists in TDR-based measurements.

TDR vs VNA comparison

Mismatch Line Device #1 Insertion Loss S21 (Magnitude dB)



TDR vs VNA comparison



Page 31



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N1024A TDR Calibration Kit

Best for Differential normalization
2 x Loads and 2 x Shorts



	Current 54754A-100	N1024A
Accessory Kit	3 36" SMA cables	2 36" SMA cables
	1 SMA-f load	2 3.5mm-f precision load
	1 SMA-m load	2 3.5mm-m precision load
	1 SMA-f short	2 SMA-f flush short
		2 3.5mm-m flush short
	2 SMA-m to BNC-f	2 3.5mm f-f adapter
	5 3.5mm 20dB pads	1 SMA-f to BNC-m
		1 Torque wrench

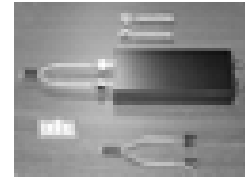
Page 32



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Diff. TDR Probe

Used for handheld Differential meas.
2 x Diff. and 2 x Single Ended Probes

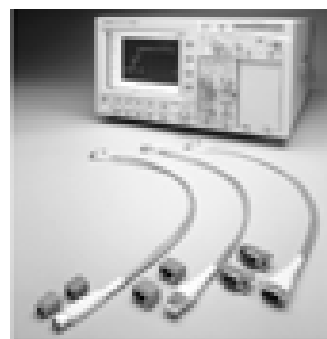


	Current 54754A-100	PS-X10-100
Accessory Kit	3 36" SMA cables 1 SMA-f load 1 SMA-m load 1 SMA-f short 2 SMA-m to BNC-f 5 3.5mm 20dB pads	2 SMA cables 2 SMA-m precision load 2 SMA-m flush short 2 Size Diff. TDR probe 2 Size Single Ended Probe 1 Calibration Subtract 1 Hand Held holder 1 ESD protection (option)

TDR Accessories

Do you know we have ;

- ┐ N1020A-K08 FireWire TDR Cable
(IEEE 1394)
- ┐ N1020A-K09 HSSDC* TDR Cable
Gigabit Ethernet (IEEE 802.3
Standard)
- ┐ N1020A-K10 DB-9 TDR Cable
Fibre Channel (ANSI x3.297-1997)

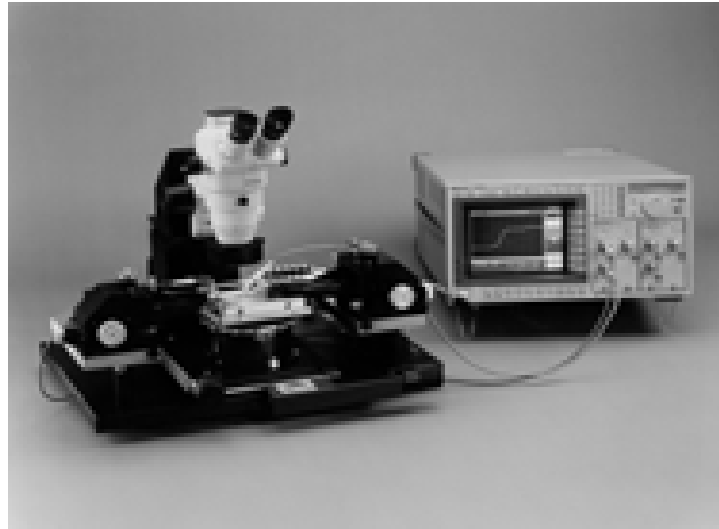


InfiniBand 1x, 4x will be available

USB2.0 & HDMI are under investigation

*** High Speed Serial
Data Connector**

On Wafer & Packages measuring example

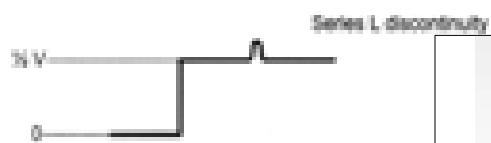


Page 35

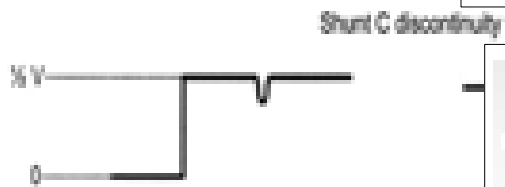
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Interconnects – Using Excess L/C



$$L = \frac{1}{2} \int_{t_1}^{t_2} Z(t) dt$$



$$C = \frac{1}{2} \int_{t_1}^{t_2} \frac{1}{Z(t)} dt$$

Page 36

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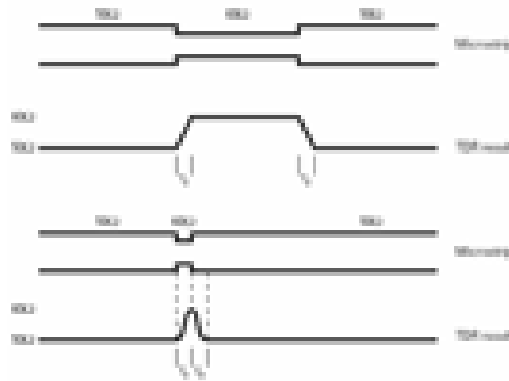
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How close can two reflection sites be and still be seen as independent events?

The TDR edge needs time to reach its full height before the next event is encountered

So what determines the two-event resolution?

Answer: It's not just the TDR step speed!



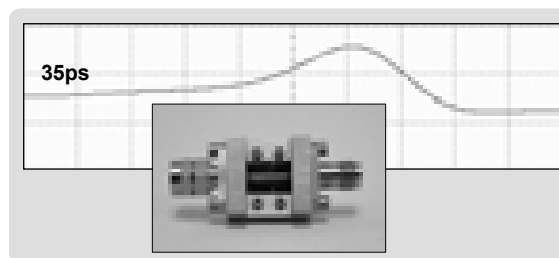
Page 37

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A 35 picosecond step is insufficient to see closely spaced reflections

With a 35 ps step, all you know is the device is there
If there is more than one reflection, we can't tell

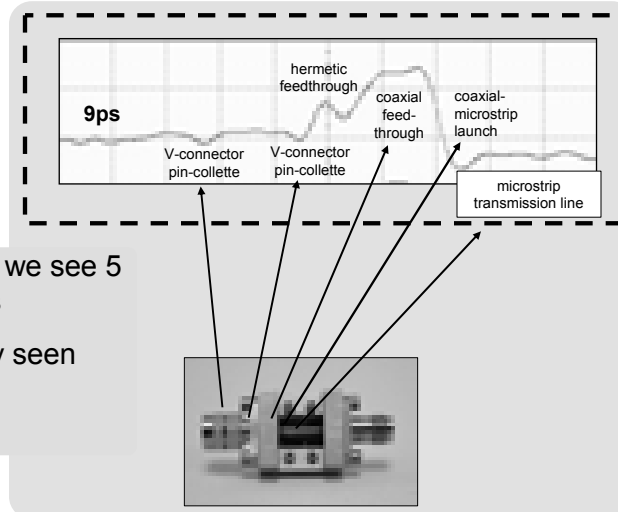


Page 38

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High resolution allows your customers to see what they could never see before



At 9 ps step speed, we see 5 separate reflections

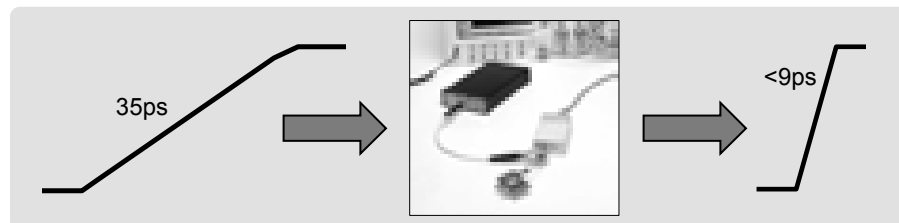
Each event is easily seen and quantified

86100/Picosecond Pulse Labs 4020/4022 Measurement capabilities

The Picosecond Pulse Labs 4020 modules takes the 35 Picosecond pulse from the Agilent TDR and increases the speed to under 9 picoseconds

Two-event resolution is improved by a factor of 4!

(1.5 mm 'air', less than 1 mm in common dielectrics)



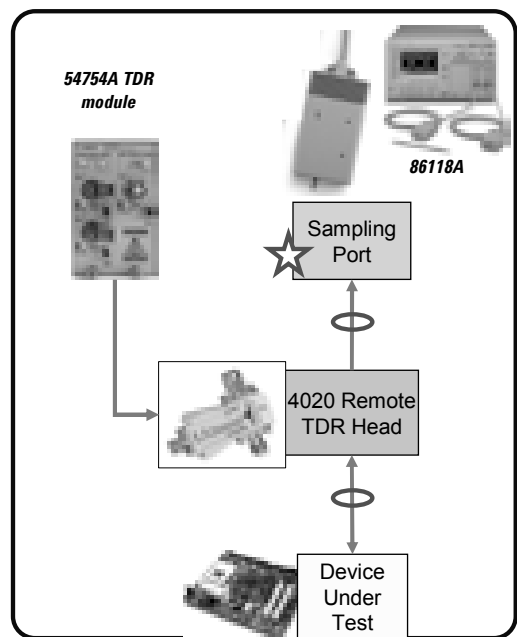
Optimizing Measurements

You will lose your edge speed if you have:

- Excess or poor quality cabling to and from the DUT
- The scope receiver channel has insufficient BW

Recommend TDR with the 86118A ~75 GHz remote plug-in:

- Max. bandwidth
- Minimum cabling distances
- Connector recommend as 2.4mm



Configuring a system

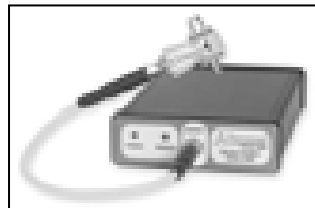
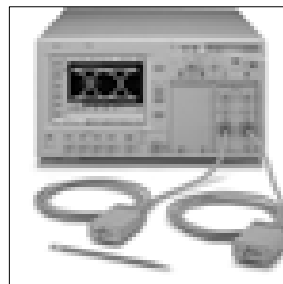
86100 C mainframe

54754A TDR plug-in

86118A 70 GHz plug-in

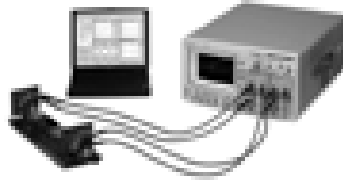
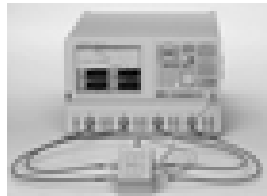
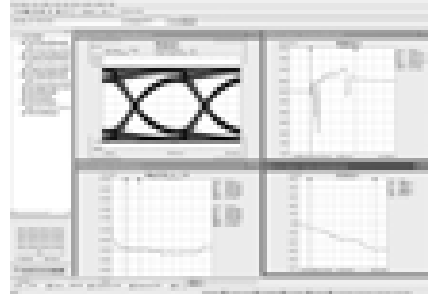
- Lower BW channels can be used, but edgespeed and resolution will be reduced
- Cabling between the DUT and the receive channel degrades TDR speed

Picosecond 4020 (Single-end) or 4022 (differential) TDR or TDT enhancement module



Physical Layer Test System (PLTS) is the Most Complete for Differential S parameters

- Extensive Calibration
- Eye diagram simulation
- N5320A-225 20G VNA
- N5320A-240 20G VNA
- 54754Ax2 TDR base



Thanks

Q & A

Using ADS for Signal Integrity Design



Signal Integrity and
Advanced Design System

Agilent Technologies Ltd.

Ming Chih, Lin
Application Engineer
Feb, 23, 2006

Overview

Part I

- Unified Environment for SI Design

Part II

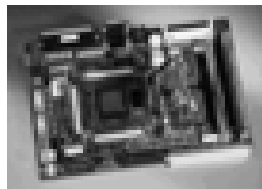
- Application Guides for SI
- Eye Diagram
- IBIS Model
- Momentum

Using ADS for Signal Integrity Design

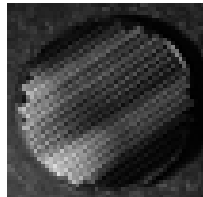
Unified Environment for SI Design

Signal Integrity Problems are Everywhere!

Backplanes



Wafers



PC Boards



IC Packages



Cables



Signal Integrity (SI)- What is it?

"Signal integrity is a field of study half-way between digital design and analog circuit theory"

Dr. Howard Johnson

It is the application of engineering principles to:

Control impedance and reflections

Minimize parasitic and unwanted coupling effects

Control skew

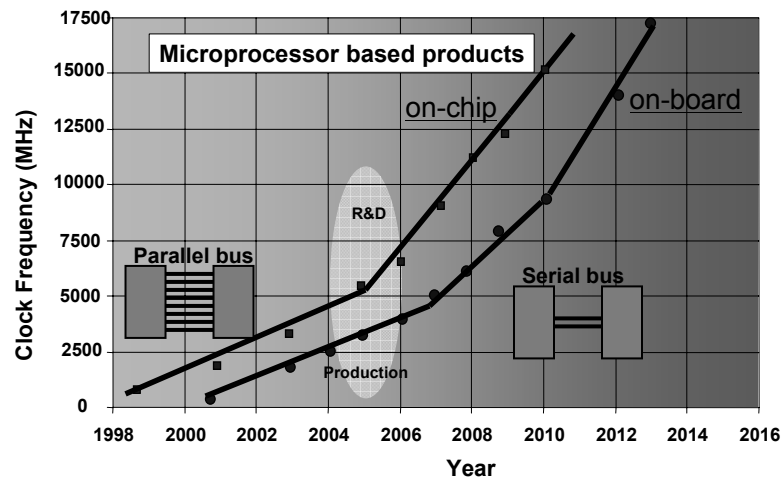
Adjust for skin-effect and dielectric losses

Transmitter Pre-emphasis

Receiver Equalization

So chips can communicate at higher data rates

Projected Increase of Clock Frequencies



Source: ITRS 2003 SIA Roadmap

Computer Interconnect Standards



Page 7



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High-Speed Signaling Standards

Standard	Data Rate (Gb/s)	Driver Edge Rate (ps)	Receiver Sensitivity	Receiver Eye Opening or Setup/Hold
Serial				
PCI Express (3GIO)	2.5	50ps to 140ps	200mVpp to 400mVpp	100ps to 140ps
RapidIO Serial	3.125			
10GbE XAUI	3.125			
Fibre Channel 2125	2.125			
Infiniband	2.5			
Serial ATA	1.5			
Parallel				
RapidIO 8/16	2			
HyperTransport	1.6			

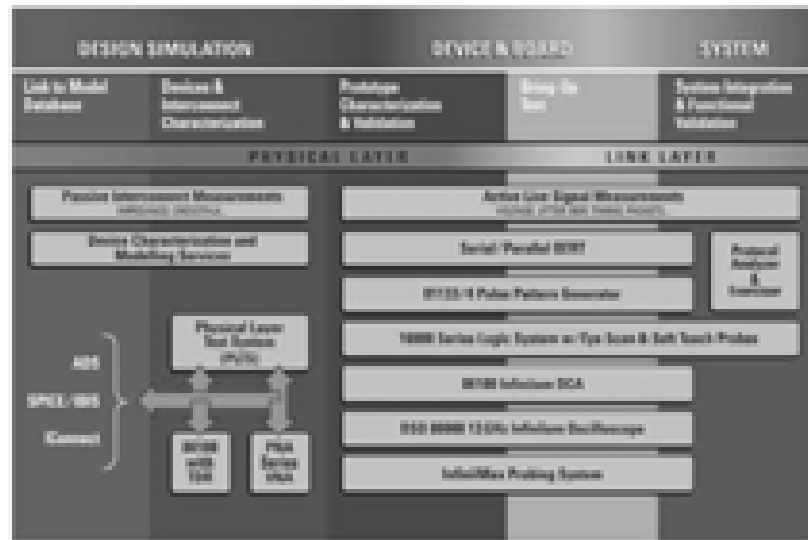
- ✓ Edge rates are decreasing below 100ps
- ✓ Differential voltage swings are shrinking
- ✓ The model bandwidth required for accurate measurements is primarily dependent on the signal's risetime, not its data rate.

Page 8



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Agilent's Signal Integrity Solutions

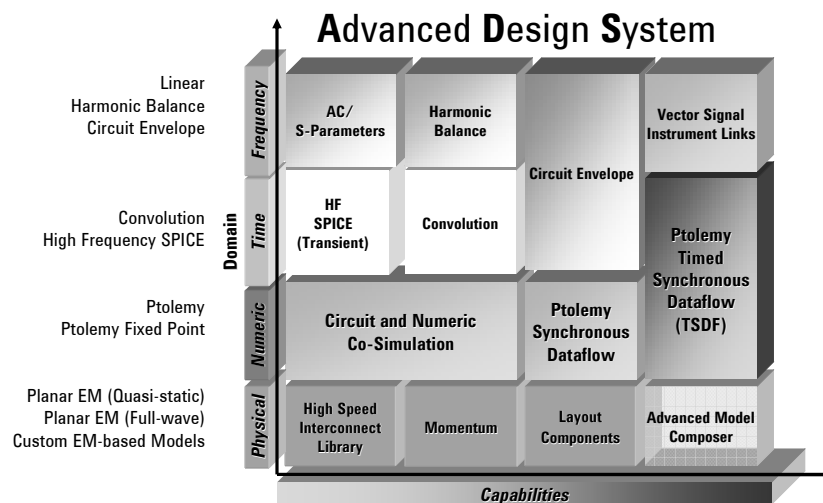


Page 9

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Simulation Leadership

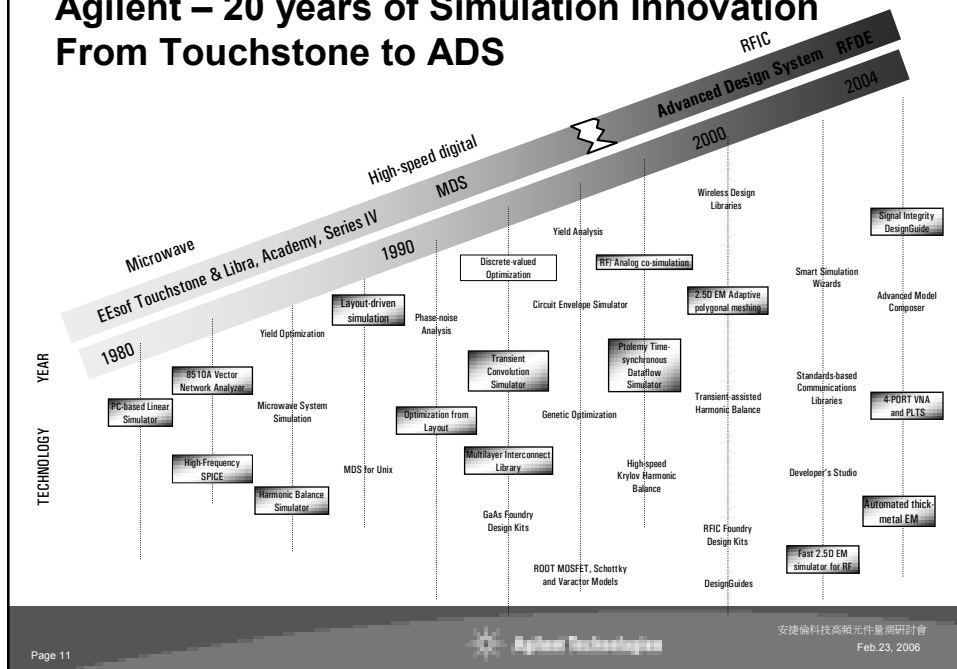


Page 10

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Agilent – 20 years of Simulation Innovation From Touchstone to ADS



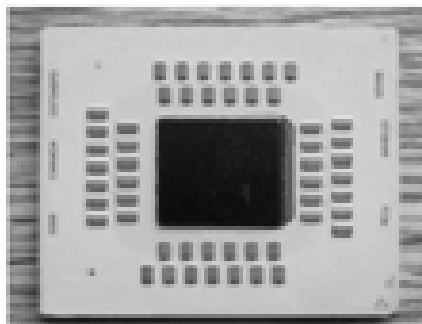
Page 11

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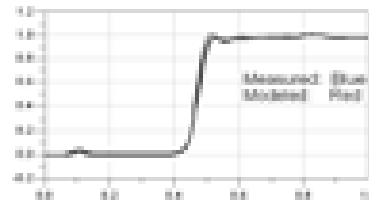
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ADS for Signal Integrity

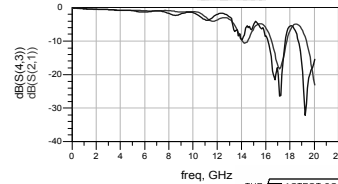
1924 pin LTCC Package Designed using ADS



Measured vs Modeled, 50 ps TDT response



Measured vs Modeled, Insertion Loss (S21)



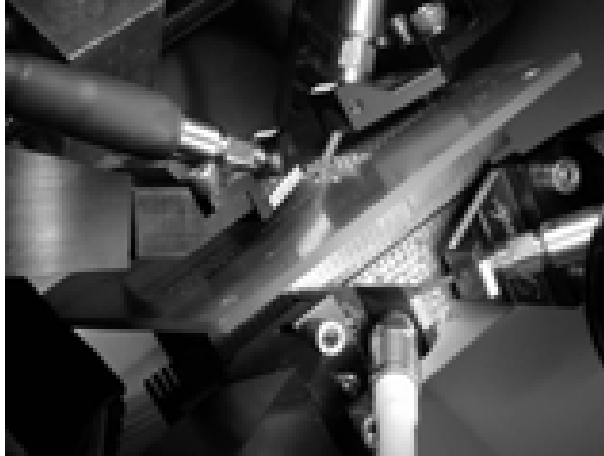
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Page 12

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4-port Measurement of Connector



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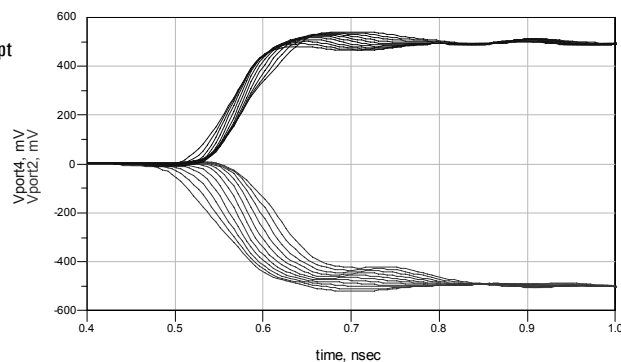
Page 13

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Simulated Step-response of Measured Connector

- Differential pair simulated their response to a voltage step.
- Main through line is held fixed during simulation
- The complement line is swept from ± 50 ps
- magnetic effect in board is evident in measurement.

differential, true/complement skew ± 50 ps.
Both output steps shown Below.



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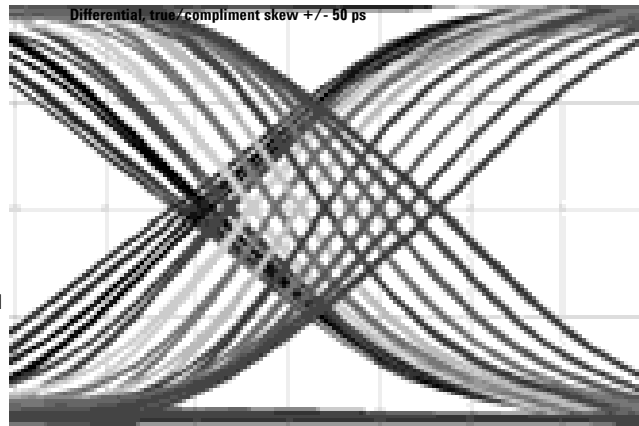
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Page 14

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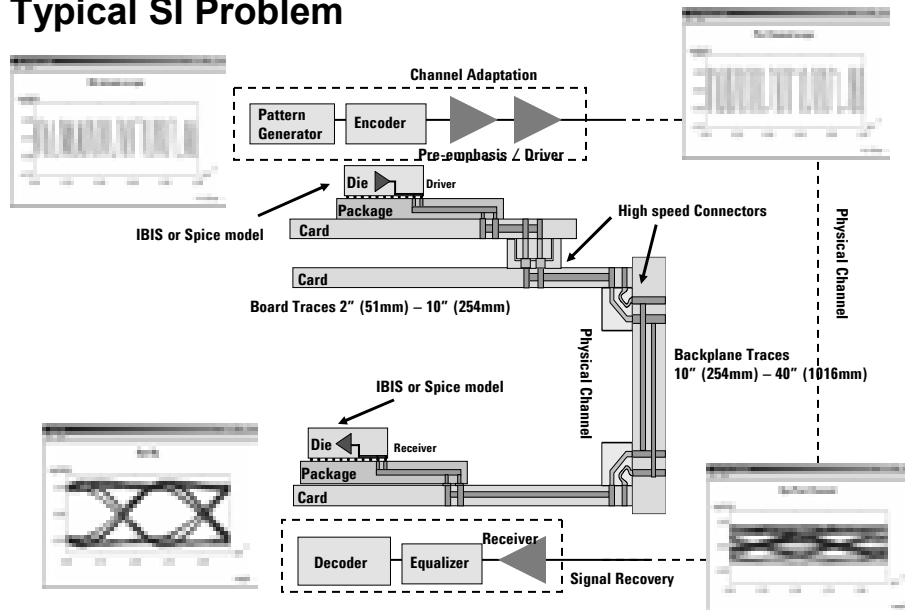
Simulated Eye Diagram of Measured Connector

- Eye opening on left-side is smaller than on right-side of crossing point for -50, -40, -30ps.
- Jitter is higher for -50, -40 and -30 ps eyes
- Slope of rise is shallower for + and - 50 ps eyes
- Eye opening is balanced and rise is faster for 0, +10 and +20ps
- Physical line added to board to adjust delay based on these results



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Typical SI Problem



ADS for Signal Integrity – Link Level Simulation

Simulators

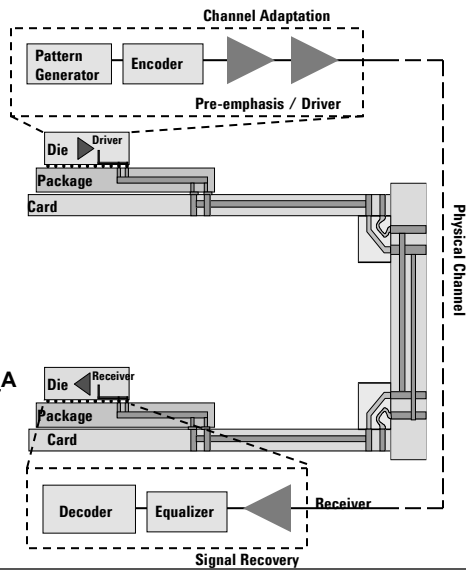
- Frequency-domain
- Time-domain
- Numeric Domain
- 3-D Planar Electromagnetic
- 3-D Electromagnetic

Models

- Optimized equivalent circuit models
- Analytic transmission line models
- Static field-solver based models
- EM simulation models
- Models from measurements
- Matlab, VHDL, C++, SystemC, Verilog_A

Measurements

- TDR and TDT
- 2-port and 4-port VNA
- Eye Diagram



Simulators - Solve the Whole Problem

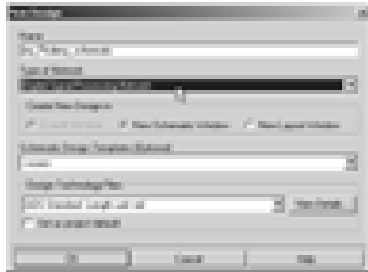
Each part of the Link can be modeled and designed separately, however...

What happens when the parts are brought together for the first time?

Would it be beneficial if the Link could be analyzed as a whole?

Agilent Ptolemy

- Agilent Ptolemy is the Data Flow simulator
- System Level Simulation Kernel
- based on UC Berkeley Ptolemy
- Timed Synchronous Data Flow (TSDF)
- Numeric Synchronous Data Flow (SDF)
- Links to other simulators & instruments

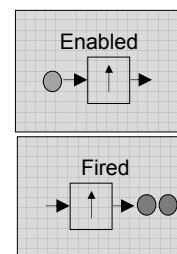


Ptolemy Data Flow (discrete numeric/time-domain)

- Signal Processing Verification – FEC, Encoding/Decoding
- System Performance Verification – uncoded/coded BER

What is Synchronous Data Flow (SDF)?

- **Statically Scheduled Simulation**
 1. A component maps input tokens (current or numbers) onto output tokens
 2. A set of firing rules specify when a node (component) runs
 3. A firing consumes input tokens and produces output token
 4. Nodes (components) connected by arcs (wires)
 5. Schedule is constructed once and repeatedly executed
- **Suitable for synchronous multi-rate signal processing**
- **Synchronous Data Flow has no concept of time, just numeric data**
- Tokens can also be “time stamped” - then they become samples. Now you can simulate time and frequency domain models and impairments such as reflections and dispersion → TSDF

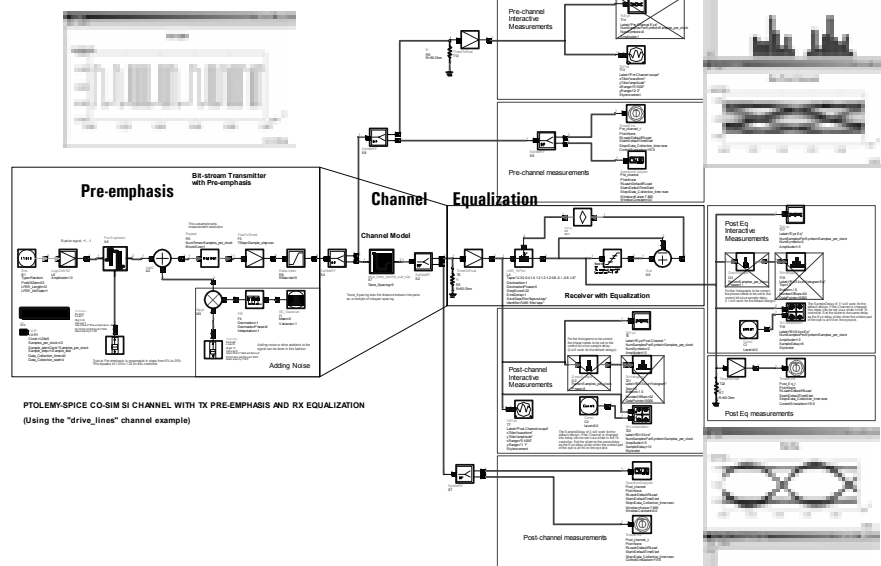


Agilent Ptolemy - The “IP Integrator”

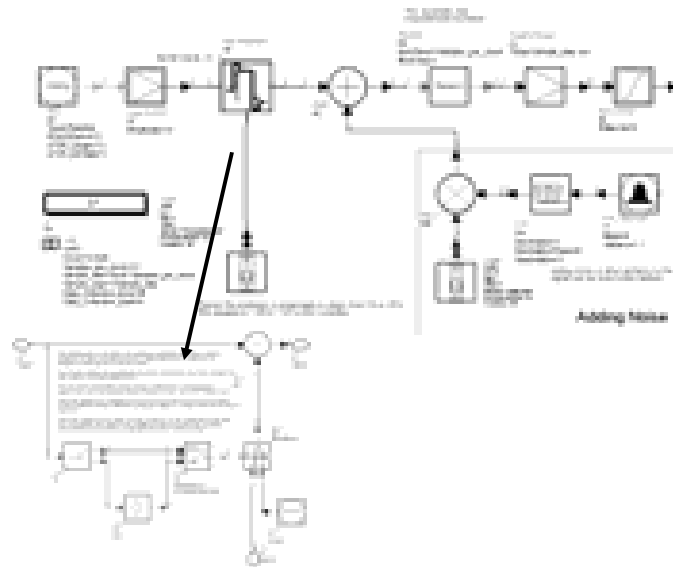
ADS Ptolemy is a solution for the following:

- Design & verification of Communication Systems (physical path).
- Co-Simulation of Baseband (DSP) and Analog/RF (A/RF) circuits in a single simulation:
 - Ptolemy system with ADS circuit simulators (which can also contain Verilog-A models).
 - Ptolemy system with 3rd party tools (Matlab, RTL-HDL simulators, C++, SystemC)
- “Connected Solutions” connect Simulation, Design & Verification flows to Instrumentation and Measurements
- Circuit verification with System Test Benches (WTBs) to link ADS and Cadence (IC) design tools.

Link Level Simulation



Transmitter with Pre-Emphasis

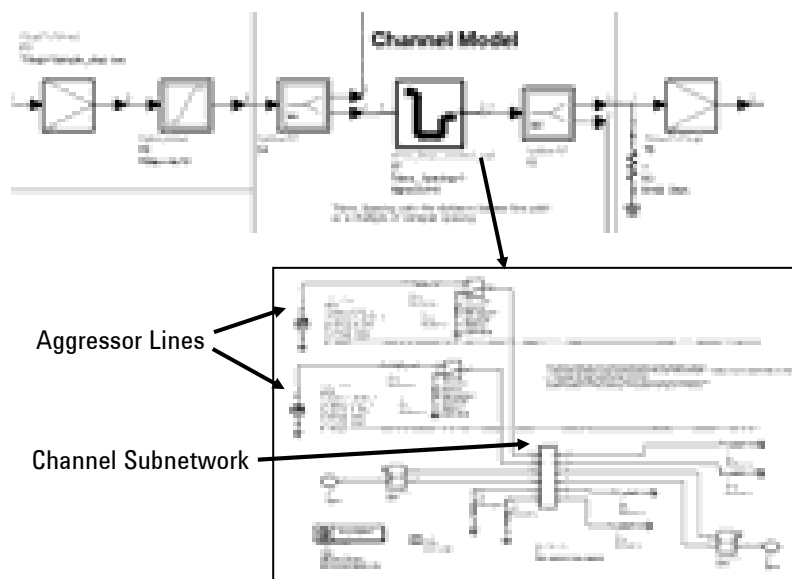


Page 23

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Channel Model

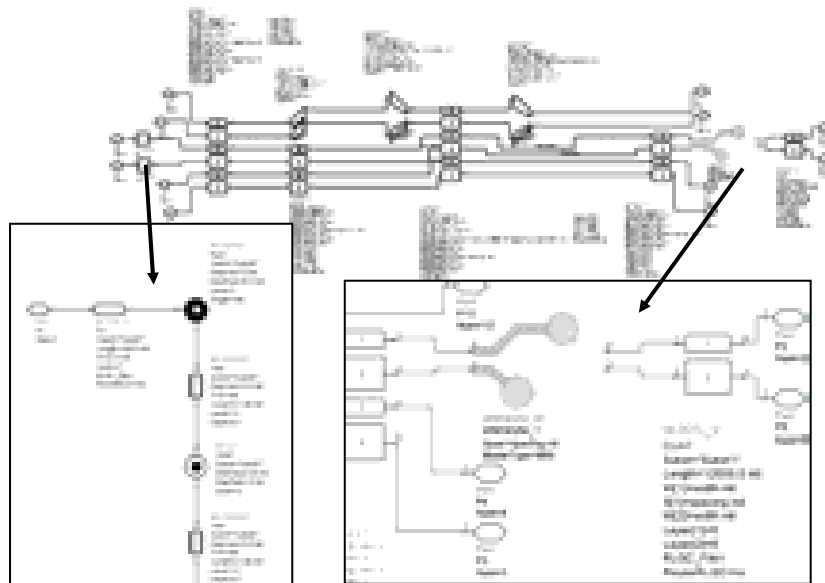


Page 24

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Feb. 23, 2006

Channel Subnetwork



Page 25

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Models



Accurate models of interconnects
+
Accurate models of the active devices
+
Accurate models of Tx and Rx Functions
+
Robust simulator
=
Accurate Prediction of performance

The earlier in the design cycle that problems are found and designed out, the shorter the cycle time, the lower the development costs

Page 26

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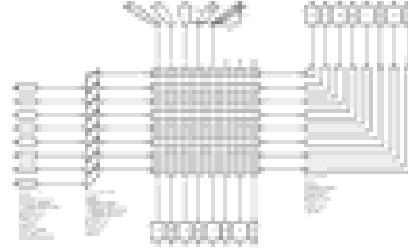
Interconnect Models

Account for impedance, delay, conductor loss, dielectric loss, and coupling

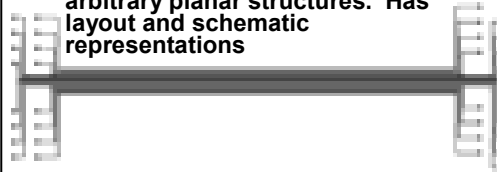
Analytic models are fast, and have a layout and schematic representation



Multilayer Interconnect Models use a built-in field-solver, and have both layout and schematic representations



Momentum EM simulator for arbitrary planar structures. Has layout and schematic representations



Page 27

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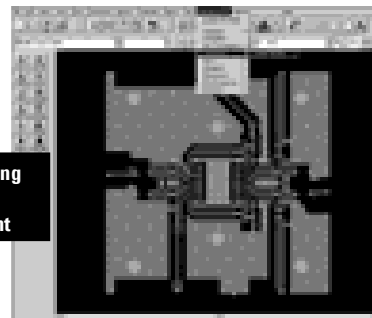
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EM Models - Momentum

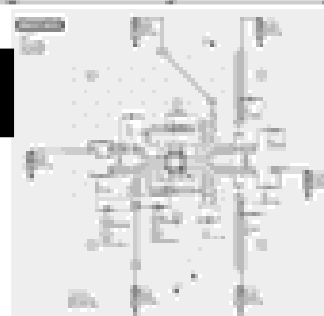
Current ADS Capabilities

- Integrated Momentum EM Simulator
- Momentum RF
- Model Composer
- Co-Simulation w/Layout Components
- Co-Optimization w/Layout Components
- Layout lookalike components

Layout editing
and port
assignment



Layout look-alike
component in the
schematic



30 GHz transition

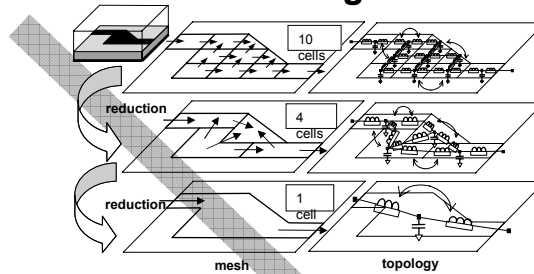


Page 28

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Momentum RF Quasi-Static Electromagnetics



Mesh strips, Vias and slots with rectangles and triangles (conformal surface mesh)

Performs mesh reduction while maintaining integrity of solution

Model surface current in each mesh cell (linear distribution)

Solve matrix equation for the unknown current coefficients

Calculate S-parameters

$$[Z] \cdot [I] = [V]$$

$$[S]$$

Low Frequency approximation :

$$e^{-jk|\mathbf{r}-\mathbf{r}'|} \approx 1 - jk|\mathbf{r}-\mathbf{r}'|$$

Electro- and magnetostatic Green's functions

Quasi-static frequency scaling ($j\omega$, $1/j\omega$)

L's and C's are real and frequency independent

R's are complex (DC loss + skin effect $\sqrt{\omega}$)

[Z] matrix load is frequency independent !

• near field / low freq approximation

$$L(\omega) = L_0 + L_1\omega + L_2\omega^2 + \dots$$

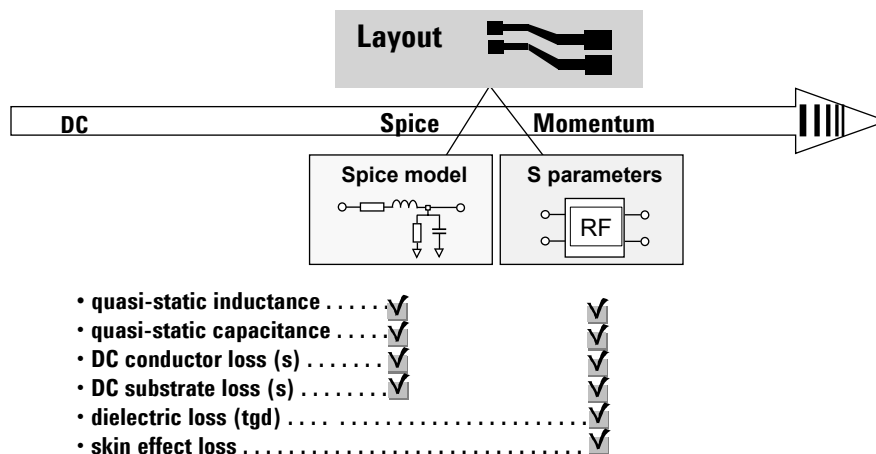
$$C(\omega) = C_0 + C_1\omega + C_2\omega^2 + \dots$$

• neglecting far field radiation

• [L₀] & [C₀] frequency independent

• [Z₀] matrix reload very fast

Comparison of Models



Models in Matlab, VHDL, C++, SystemC, Verilog-A

IP for “Link Level” blocks and functions often already exist, e.g.

- Pre-emphasis
- EQ
- Encoding/Decoding
- Interleaving/De-interleaving
- Source descriptions

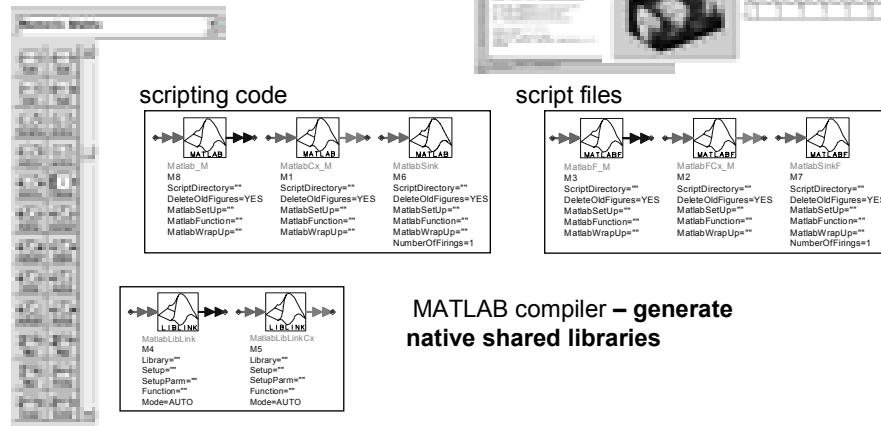
Easy to include with Ptolemy, either natively or with Co-simulation

Models - MATLAB Co-Simulation in ADS Ptolemy

Co-simulate with Matlab in ADS

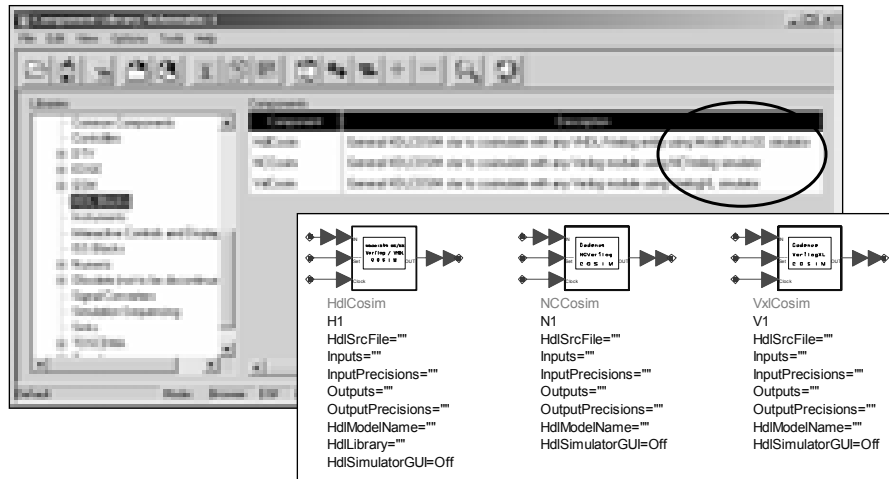
Use full Matlab UI or as math function only

Components in “Numeric Matrix” library



Models - HDL Co-Simulation in ADS Ptolemy

In the *HDL Blocks* library



Page 33



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Integration of other Models

C++ Based Model Creation and SystemC

C++

- Native Language for Ptolemy Kernel
- Model Development Through GUI and Command Line Interface
- Full Debug Capability Through 3rd Party Development Environments
 - Microsoft Visual Studio for PC Platforms



SystemC

- Application Note 1482: Importing SystemC Designs into Advanced Design System
- <http://eesof.tm.agilent.com/pdf/5989-0234EN.pdf>

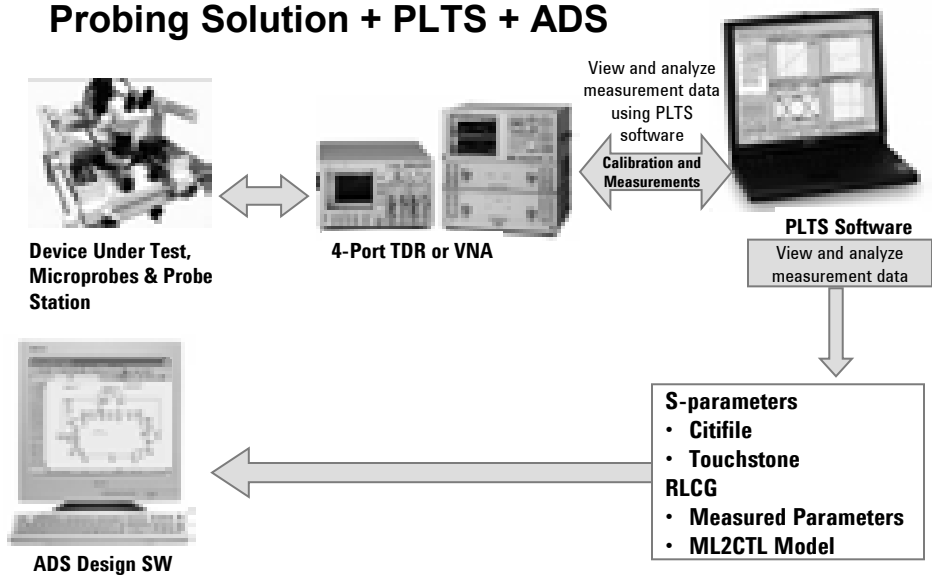


Page 34



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Measurement-based Models Probing Solution + PLTS + ADS



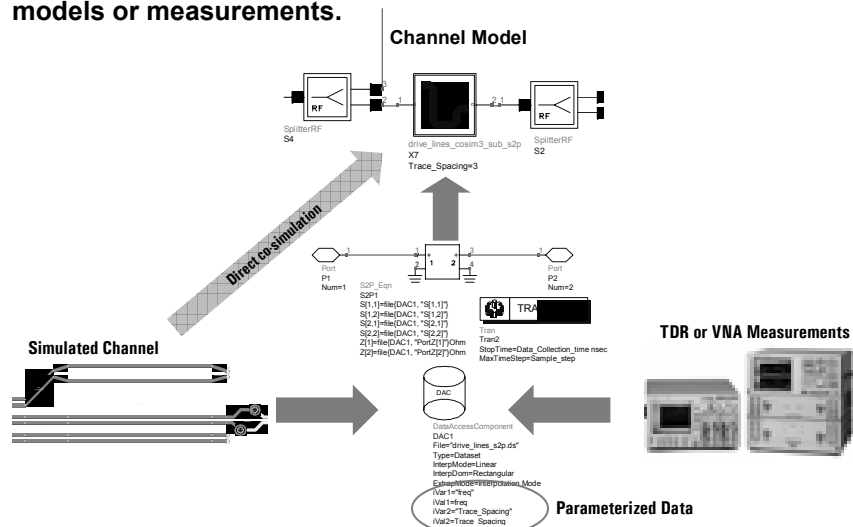
Page 35

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Link Level Simulation

Data based Channel Models can be derived from simulation models or measurements.



Page 36

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Bringing it All Together

- ADS has been used for SI design for over 10 years
- ADS can act as a scalable design whiteboard
- ADS encourages you to be curious about your design ideas
- ADS has a multitude of accurate built-in models
- ADS allows you to build accurate physical models
- ADS lets you use your existing models
- ADS agrees with measurements
- ADS shows results the way you want to see them
- ADS brings IP, simulations and measurements together
- ADS Ptolemy lets you work with the whole Link before you build it!

Signal Integrity Resources

Gigatest for probe stations and
package modeling services
www.GigaTest.com



CST for 3D EM Simulator
www.cst.com



Fastest, Inc for designing high speed
hardware and resolving signal
integrity problems.
www.fastestco.com



Admos for active and passive model
extraction services
www.admos.com

SI Resources on the Agilent EEs of website

Agilent EEs of EDA home page
<http://eesof.tm.agilent.com>

Signal Integrity Applications and Wireline Applications
http://eesof.tm.agilent.com/applications/signal_integrity-b.html
<http://eesof.tm.agilent.com/applications/wireline-b.html>

Momentum
<http://eesof.tm.agilent.com/products/e8921a-a.html>

Agilent Signal Integrity eSeminar Series
www.agilent.com/find/sigint

NetSeminar: Challenges of Differential Bus Design -
http://eesof.tm.agilent.com/news/news400.html#bus_design

Application Web site for 2005A

http://eesof.tm.agilent.com/applications/signal_integrity-b.html



Signal Integrity Training Class

<http://www.agilent.com/find/education>

Signal Integrity Class: N3215A Designing for Signal Integrity with ADS

- Transient Simulation Setup
- Convolution and Frequency-Domain Simulations
- Transmission Lines, Crosstalk and Resonances
- TDR/TDT
- Noise and Jitter
- 2.5D EM Simulations (Momentum)
- Differential Circuits and Mixed-Mode S-Parameters

— Length – 2 days – hands-on

Ptolemy training: N3206A Signal Processing using ADS

- Ptolemy SDF / TSDF
- Co-simulation
- Length – 3 days – hands-on

Using ADS for Signal Integrity Design Models, Simulations and Measurements



Using ADS for Signal Integrity Design

Application Guides for SI

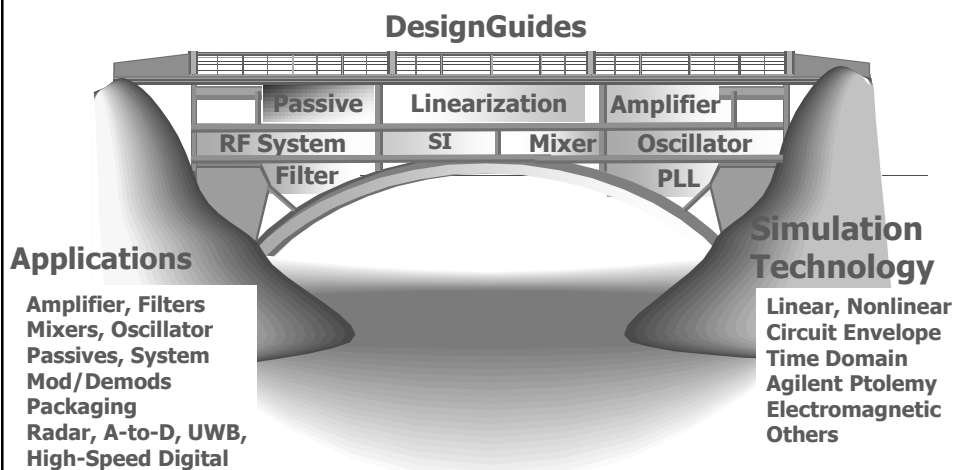
Page 43



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DesignGuides in ADS – Bridging the Gap



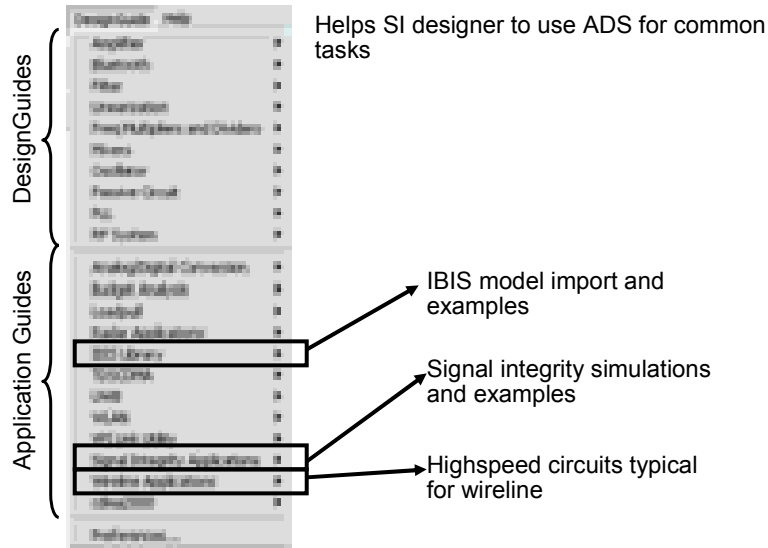
Page 44



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DesignGuides / Application Guides

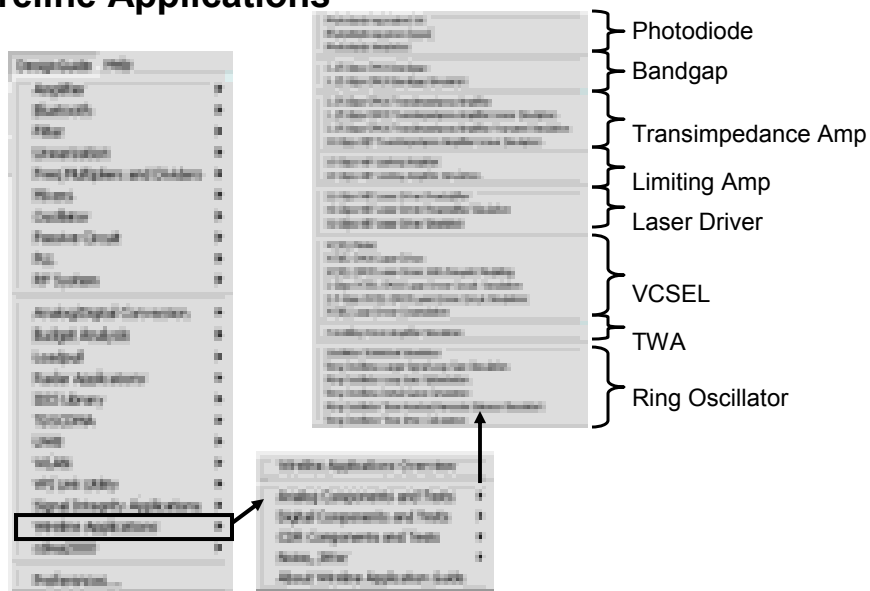


Page 45



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Wireline Applications

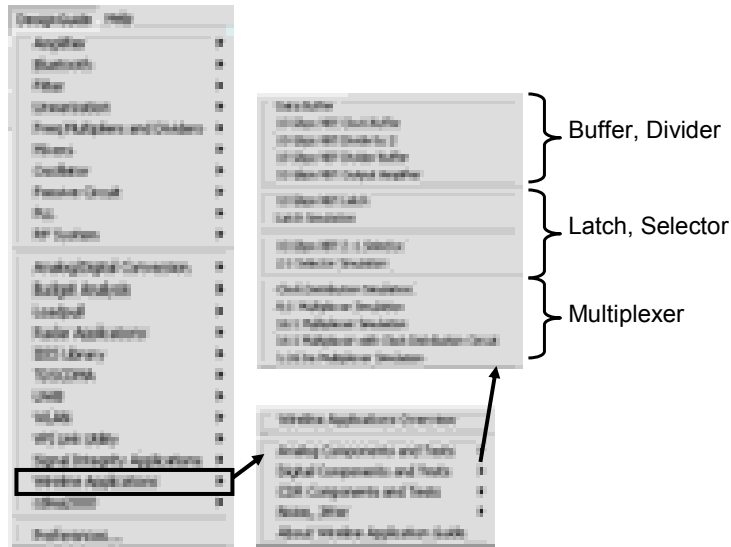


Page 46

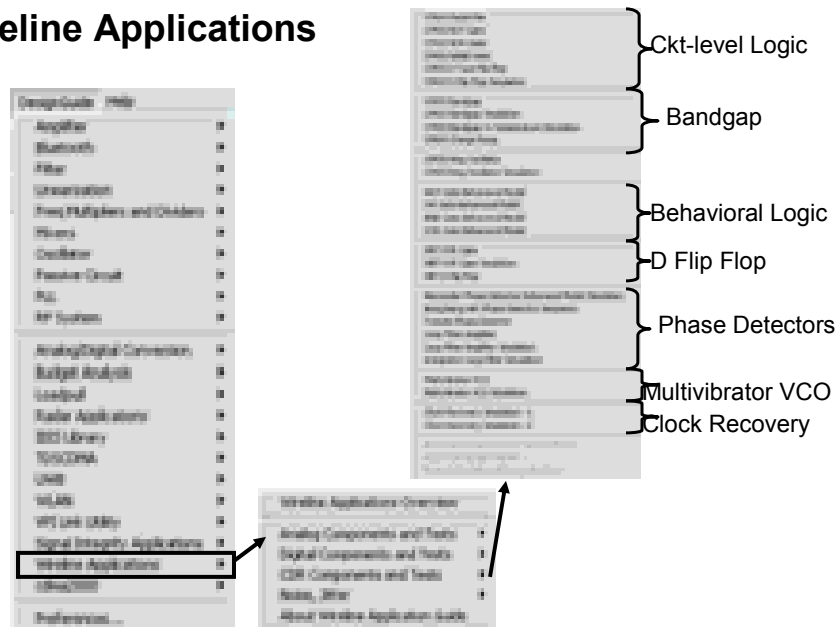


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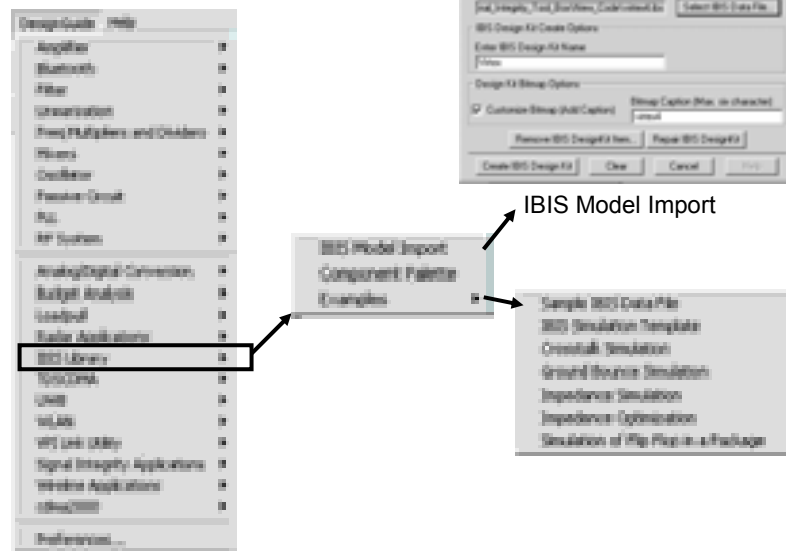
Wireline Applications



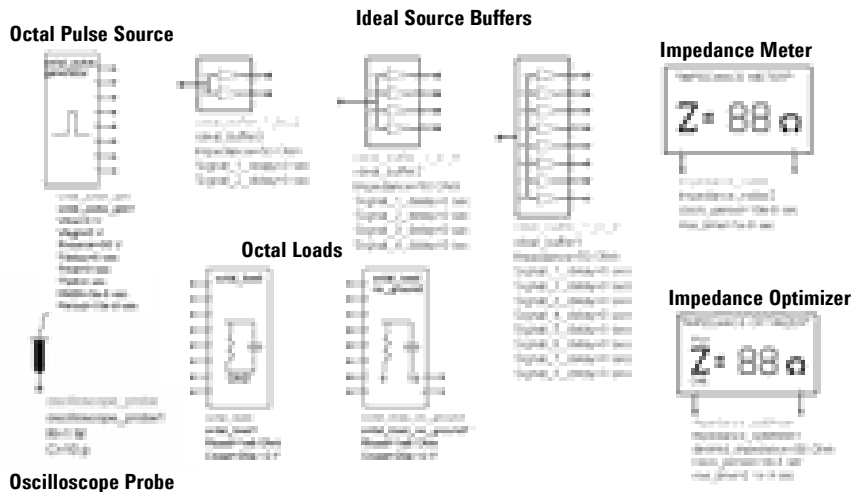
Wireline Applications



IBIS Library



Components from the IBIS Library Component Palette

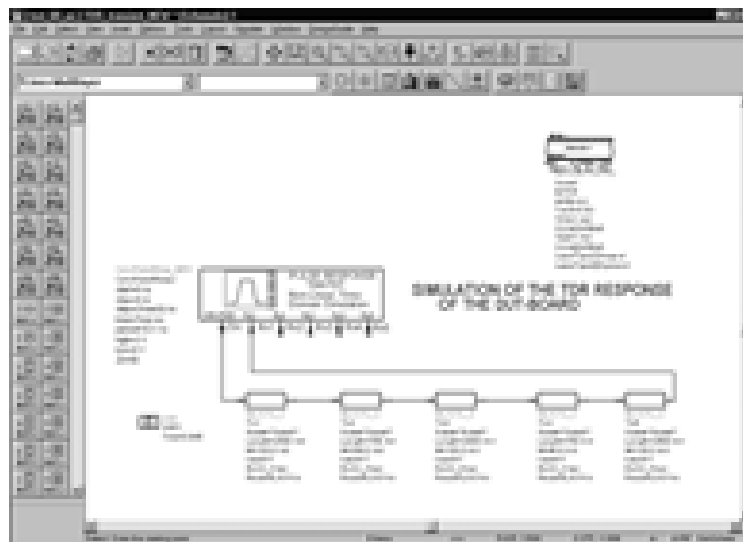


Signal Integrity Applications

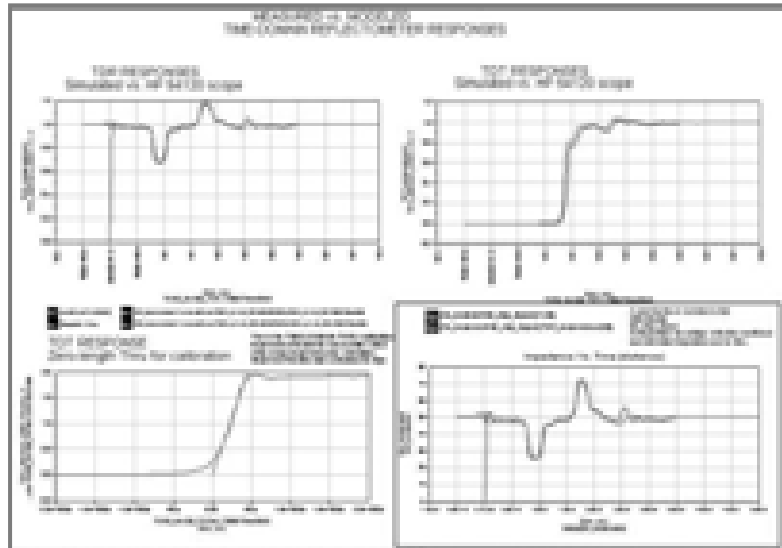
Signal Integrity Applications

- Eye Diagram measurements including jitter, FrontPanel and DCA file import
- Single Ended TDR/TDT
- Linear/Nonlinear Differential TDT
- Mixed Mode S-Parameters
- Impedance Simulations
- Pre-emphasis and Equalization

TDR Simulation Instrument



TDR Responses Using Time-domain Simulation

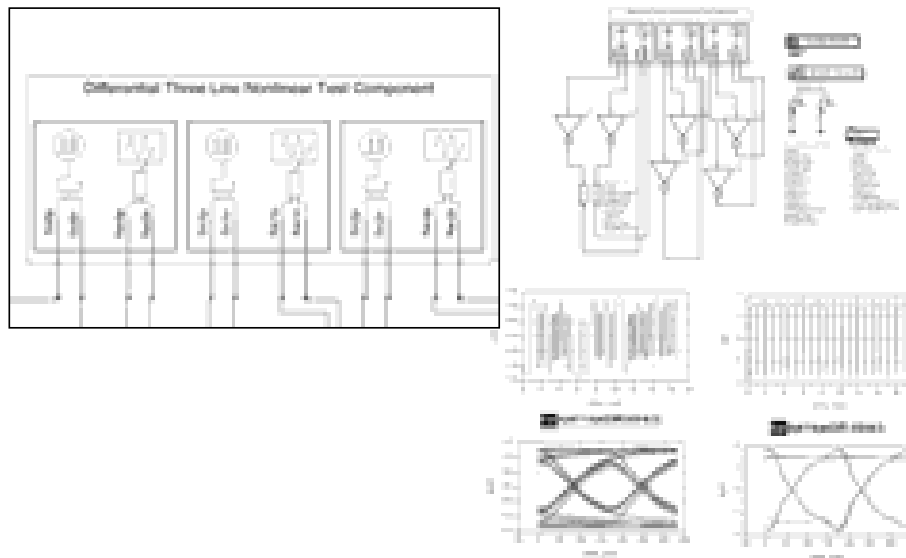


Page 53

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Differential Nonlinear Test Component



Page 54

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Using ADS for Signal Integrity Design Eye Diagram

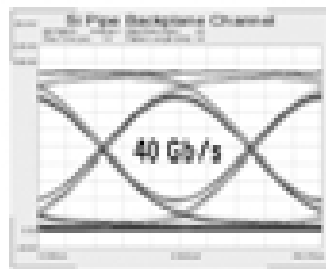
Qualitative vs. Quantitative: How close are these waveforms?

"This 40 Gb/s eye diagram was then compared to the 40 Gb/s eye diagram derived from the internal PLTS eye diagram generating algorithms.

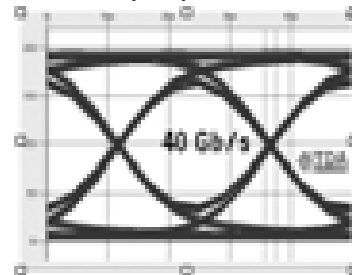
The qualitative correlation of these two simulated eye diagrams was very good."

DesignCon 2004 paper "Utilizing TDR and VNA Data to Develop 4-port Frequency Dependent Models for Simulation" Mayrand, Resso, Smolyansky

PLTS
Eye



Measurement

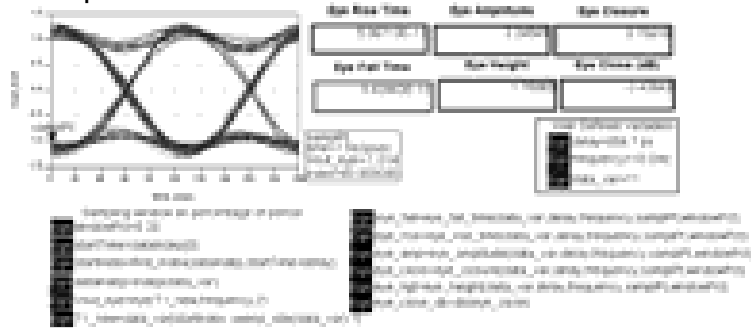


Models

Data Display strengths and weaknesses

Data Displays are flexible but require extensive use of equations and a lot of user expertise.

Some measurements are calculated, but most characteristics are left up to the user to determine.



Page 57

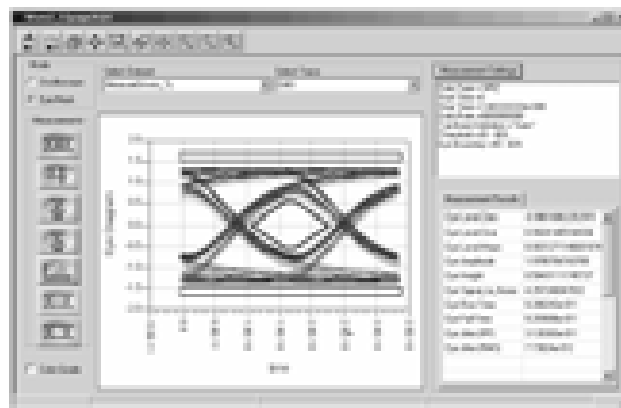
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FrontPanels: Eye Diagram

Convenience – dedicated display and push-button measurements focused on a common task. Provides over 30 data display pages and over 300 equations.

Consistency – measurement algorithms checked against instrumentation.

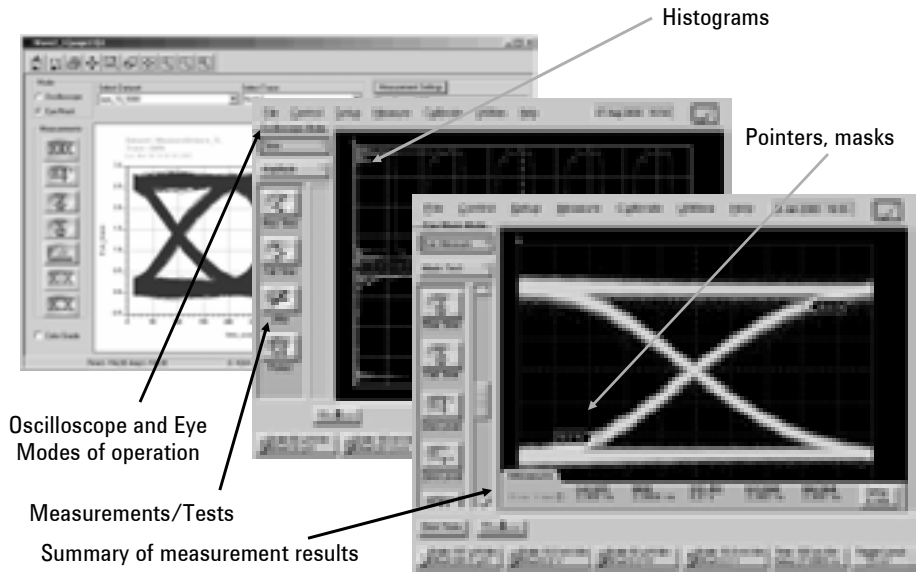


Page 58

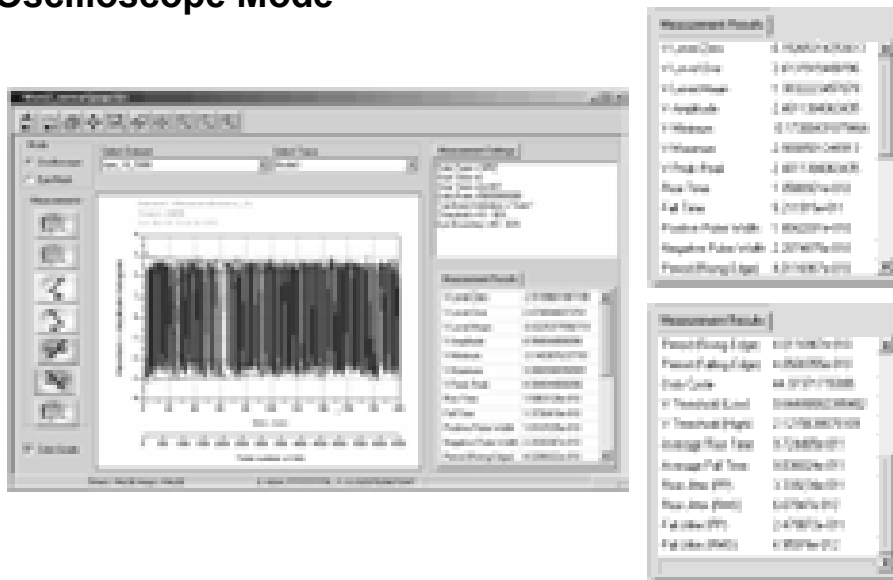
Agilent Technologies

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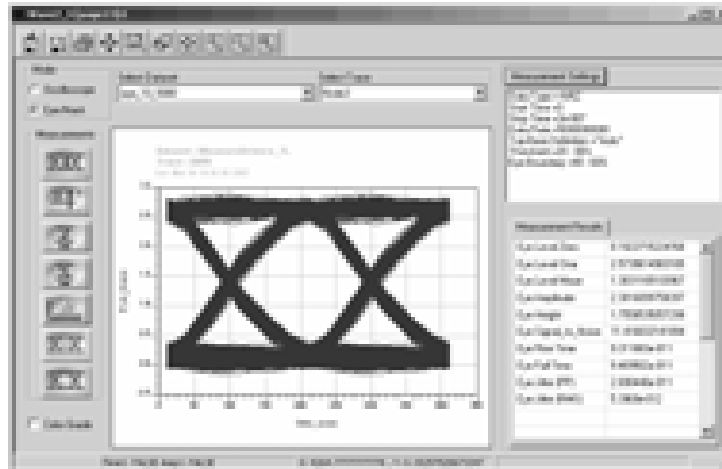
Inspired by Agilent DCA-J Instrument



Oscilloscope Mode



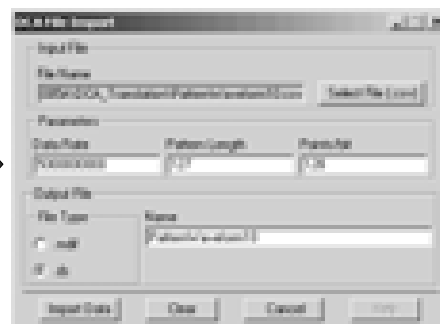
Eye/Mask Mode



Convert DCA data (*.csv format) into Dataset

Data Parser available in Signal Integrity Application Guide

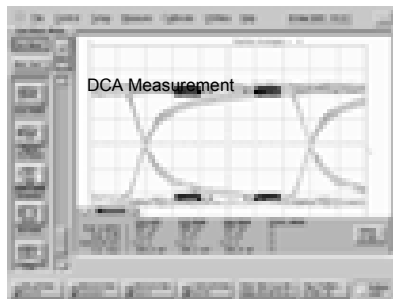
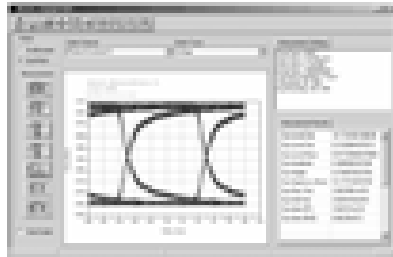
*.csv file from
DCA



Dataset file



Compare Eye FP to DCA on Same Data



1G Data Rate through 20" trace

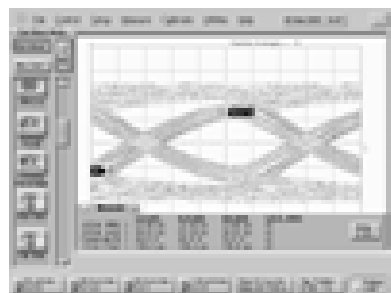
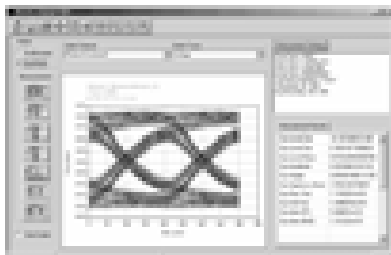
Eye Diagram FrontPanel on the DCA output file.

	FrontPanel	DCA typ	DCA
Level 1	212mV	211.3mV	211.3/213.5
Level 0	-177.4mV	-177.5mV	-177.5/-178.5
Rise Time	219pS	222pS	219/226
Fall Time	212pS	215pS	211/219
Eye Amp	389.4mV	389mV	386.3/389.4
Eye Height	274.7mV	274.7mV	273.9/274.9
Eye S/N	10.18	10.07	10.01/10.23
Jitter p-p	22.2pS	22.2pS	22.2/22.2
Jitter rms	5.8pS	5.7pS	5.7/5.8

[NOTE: FrontPanel data is from a single trace.
DCA measurements are averaged with 16 measurements.]

[NOTE: FrontPanel results are preliminary until
ADS 2005A final release.]

Compare Eye FP to DCA on Same Data



5G Data Rate through 20" trace

Eye Diagram FrontPanel on the DCA output file.

	FrontPanel	DCA typ	DCA min/max
Level 1	157mV	157.5mV	156.4/157.5
Level 0	-136mV	-136mV	-136.6/-136
Rise Time	136.3pS	136.2pS	136.2/136.9
Fall Time	140.6pS	140.6pS	140.6/140.6
Eye Amp	293.8mV	293.7mV	293.4/293.8
Eye Height	61.3mV	61mV	60.8/61.5
Eye S/N	3.79	3.79	3.79/3.80
Jitter p-p	53.44pS	54.02pS	53.28/54.02
Jitter rms	12.6pS	12.5pS	12.43/12.65

[NOTE: FrontPanel data is from a single trace. DCA
measurements are averaged with 16
measurements.]

[NOTE: FrontPanel results are preliminary until
ADS 2005A final release.]

Using ADS for Signal Integrity Design

Example Measurements

Page 65

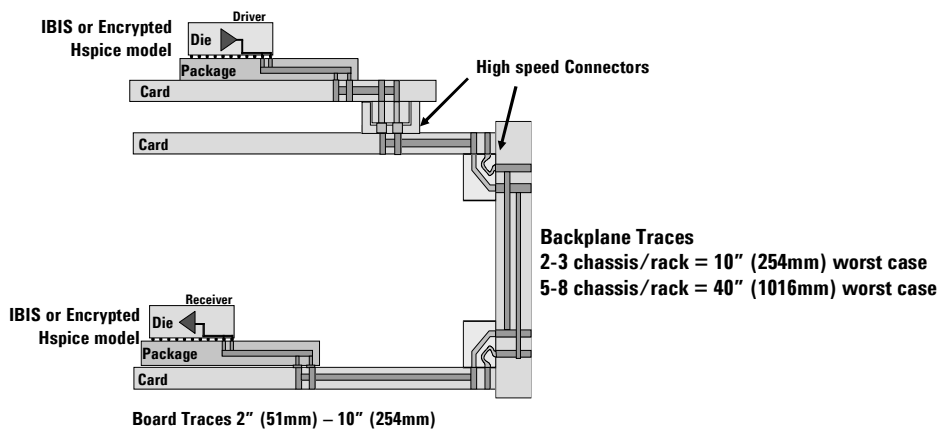


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Common SI Problem

Objective: 1m of "improved FR-4" through multiple high speed connectors.
10" (254mm) Line Card > 20" (508mm) Backplane > 10" (254mm) Line Card.
Check Eye Diagram at various points along the path.



Page 66

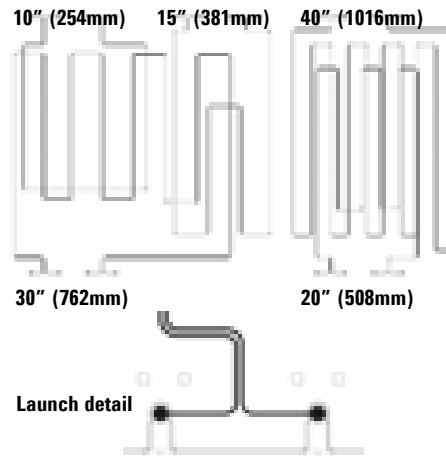
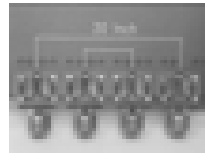
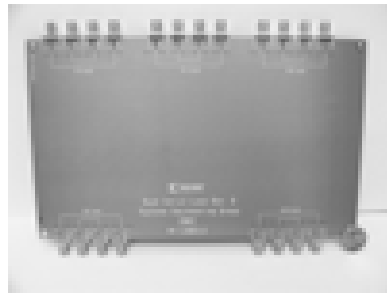


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Example Test Board

Several trace lengths on "improved FR-4" six metal layers, 62.5 mil total thickness



Page 67

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Measurements on various length of trace

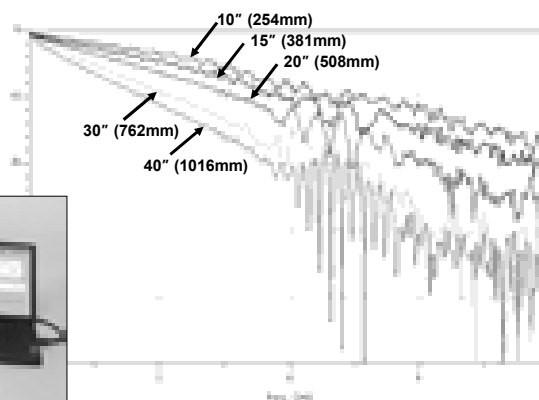
S-Parameter
measurements

Differential S-Parameter
measured with PLTS

Traces are lossy

Measurement shows
multiple reflections

Data is band limited



Page 68

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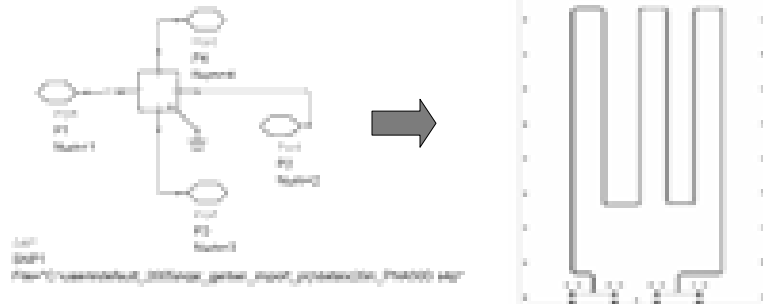
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Create Models from Data

Data-based Model

Measure with 4-port NWA

Layout Look-alike component



Page 69

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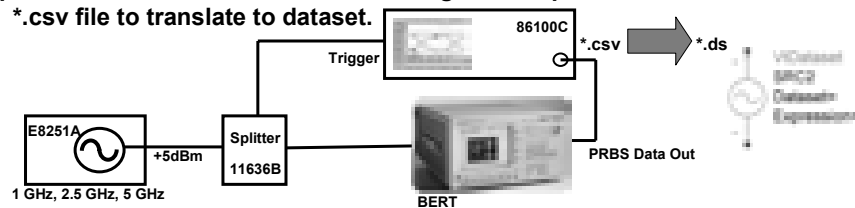
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DCA/BERT Measurement Setup

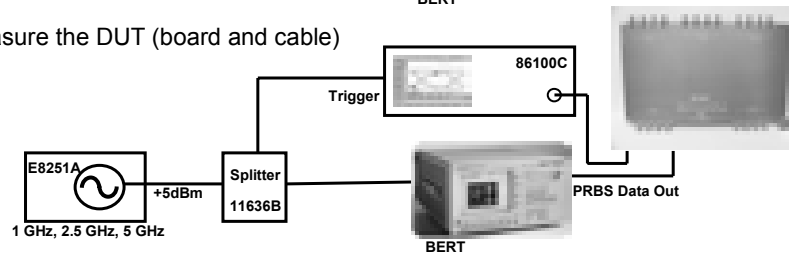
Measure the input waveform

Bypass the Board, record the waveform

Capture waveform with Connection Manager or output
*.csv file to translate to dataset.



Measure the DUT (board and cable)



Page 70

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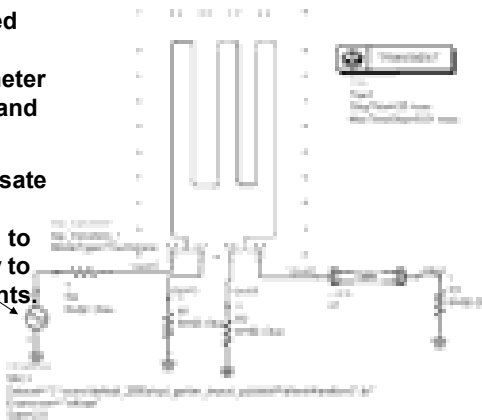
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Simulation through Measured S-Parameter Data

Simulation

Simulation of measurement-based waveform through measured S-Parameter data for the board and cable.

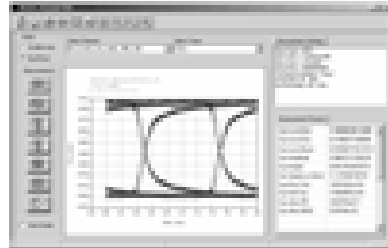
Adjust gain to compensate for loss through resistor. May need to adjust gain slightly to match measurements.



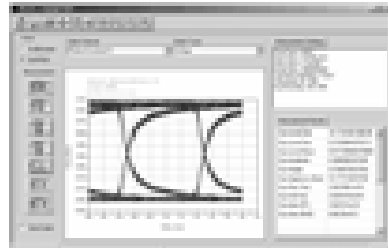
Page 71

Simulation compared to DCA Measurement

Simulation with Measured Data



DCA Measurement of BERT



1G Data Rate through 20" trace

Gain set to 1.95

	FrontPanel	DCA typ	DCA
Level 1	210.8mV	211.3mV	211.3/213.5
Level 0	-179mV	-177.5mV	-177.5/-178.5
Rise Time	197pS	222pS	219/226
Fall Time	192pS	215pS	211/219
Eye Amp	389mV	389mV	386.3/389.4
Jitter p-p	22.17pS	22.2pS	22.2/22.2
Jitter rms	5.7pS	5.7pS	5.7/5.8

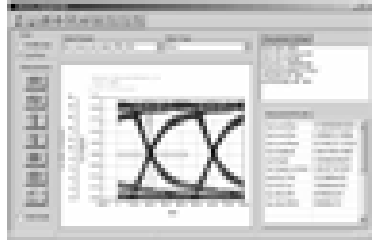
[NOTE: FrontPanel data is from a single trace.
DCA measurements are averaged with 16
measurements.]

[NOTE: FrontPanel results are preliminary until
ADS 2005A final release.]

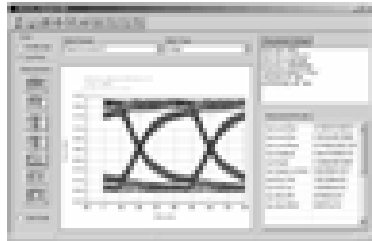
Page 72

Simulation compared to DCA Measurement

Simulation with Measured Data



DCA Measurement of BERT



2.5G Data Rate through 20" trace

Gain set to 1.90

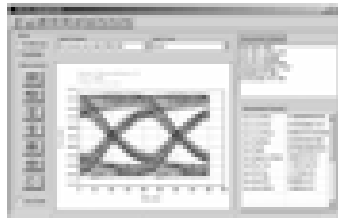
	FrontPanel	DCA typ	DCA
Level 1	187mV	186mV	188.9/188.6
Level 0	-158.9mV	-157.7mV	-158.6/-157.4
Rise Time	157.9pS	178pS	169-178
Fall Time	157.9pS	172pS	172-176
Eye Amp	346mV	344mV	344-345.8
Jitter p-p	40.8pS	37.1pS	37.1-38.5
Jitter rms	9.39pS	9.4pS	9.1-9.4

[NOTE: FrontPanel data is from a single trace.
DCA measurements are averaged with 16 measurements.]

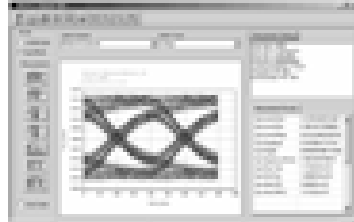
[NOTE: FrontPanel results are preliminary until
ADS 2005A final release.]

Simulation compared to DCA Measurement

Simulation with Measured Data



DCA Measurement of BERT



5G Data Rate through 20" trace

Gain set to 1.90

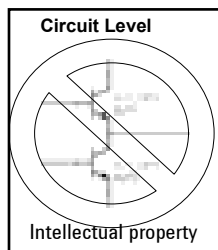
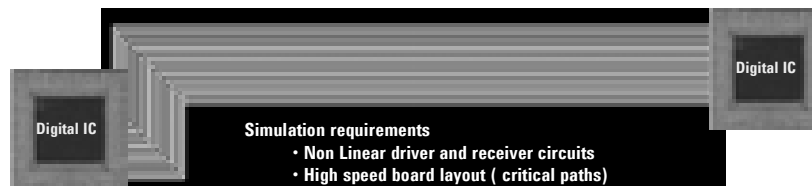
	FrontPanel	DCA typ	DCA
Level 1	155mV	157.5mV	158.9/157.5
Level 0	-137mV	-136mV	-136.6/-136
Rise Time	133pS	136.2pS	136.2/136.9
Fall Time	133pS	140.6pS	140.6/140.6
Eye Amp	292mV	293.7mV	293.4/293.8
Jitter p-p	54pS	54.02pS	53.28/54.02
Jitter rms	12.3pS	12.5pS	12.43/12.65

[NOTE: FrontPanel data is from a single trace.
DCA measurements are averaged with 16 measurements.]

[NOTE: FrontPanel results are preliminary until
ADS 2005A final release.]

Using ADS for Signal Integrity Design IBIS Model

IBIS Model



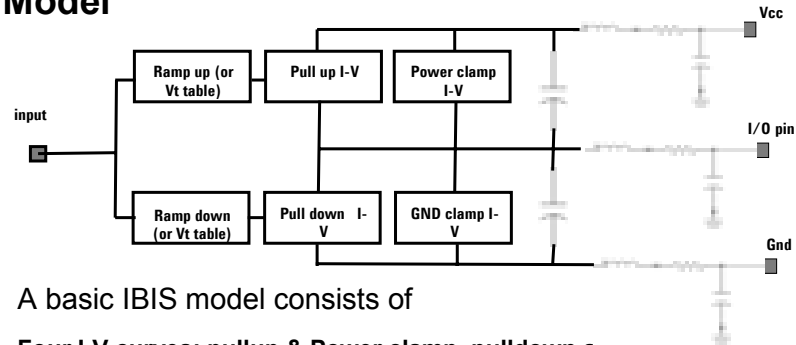
IBIS (Input/Output Buffer Information Specification) models enable IC vendors to communicate device characteristics without revealing circuit / process information.

IBIS Model

Behavioral Level

[Power_clamp]			
Note that the[POWER_clamp]voltage table is referenced to Vcc and is calculated using Vtable-Vcc - Vmeasured.			
Voltage	I(typ)	I(min)	I(max)
0.000	265.0uA	NA	NA
-0.600	368.0uA	NA	NA
-1.200	445.0uA	NA	NA
-2.050	578.0uA	NA	NA
-2.800	685.0uA	NA	NA
-3.500	788.0uA	NA	NA
-4.000	878.0uA	NA	NA
-4.500	935.0uA	NA	NA
-4.750	975.0uA	NA	NA
-5.000	1018.0uA	NA	NA
[GND_clamp]			
Voltage	I(typ)	I(min)	I(max)

IBIS Model



A basic IBIS model consists of

Four I-V curves: pullup & Power clamp, pulldown and Gnd clamp

Two ramps (Rampup and Rampdown) and/or Two/Four Vt tables

Die capacitance: C_comp

Packaging: RLC values

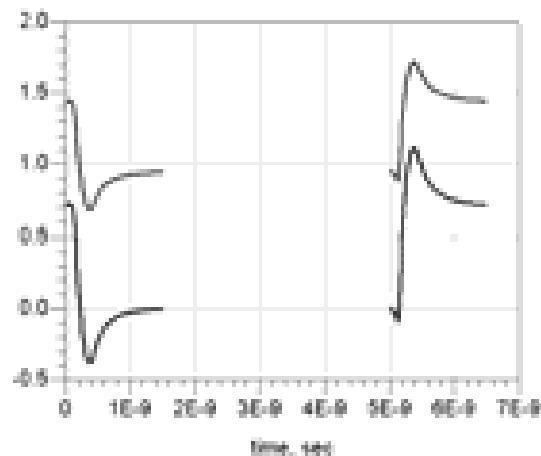
For each buffer on a chip

Page 77

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Feb. 23, 2006

**For one pair of V(t) waveform,
The other pair is created for a
different value of V-fixture.**



Red- V(t) waveform
pair in IBIS data

Blue- Synthesized
V(t) waveform
pair in IBIS data

Page 78

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Feb. 23, 2006

Comparison of IBIS model Vt table vs. Rise/Falltime

Rise/Fall Time

uses an average value of risetime/falltime to set the time constant of a capacitor.

Usable back to IBIS v1.0

Uses SDD-based equivalent circuit

Can be used in HB as well as Transient simulation

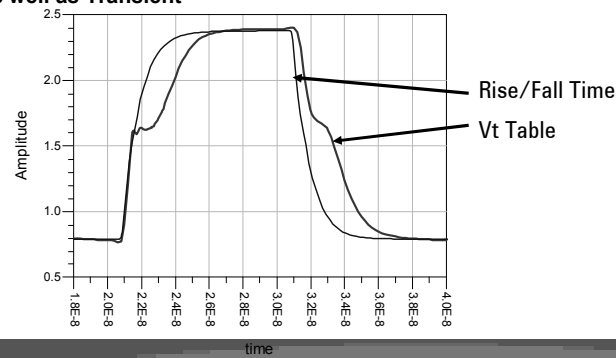
Vt Table

uses voltage lookup table (Vt)

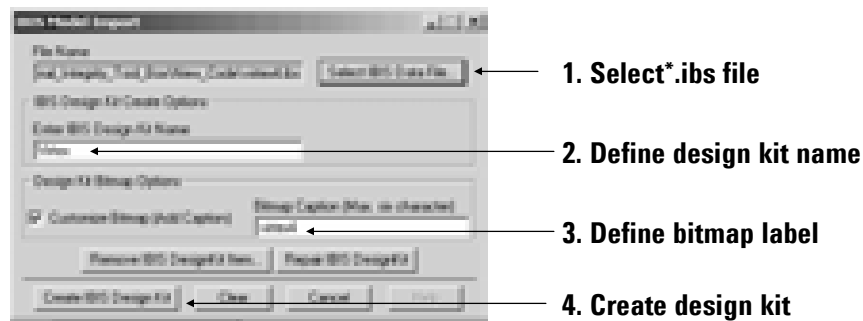
Usable starting with IBIS v2.x

Uses FDD-based equivalent circuit

Can be used only in Transient simulation



Importing IBIS Component



Installation of design kit

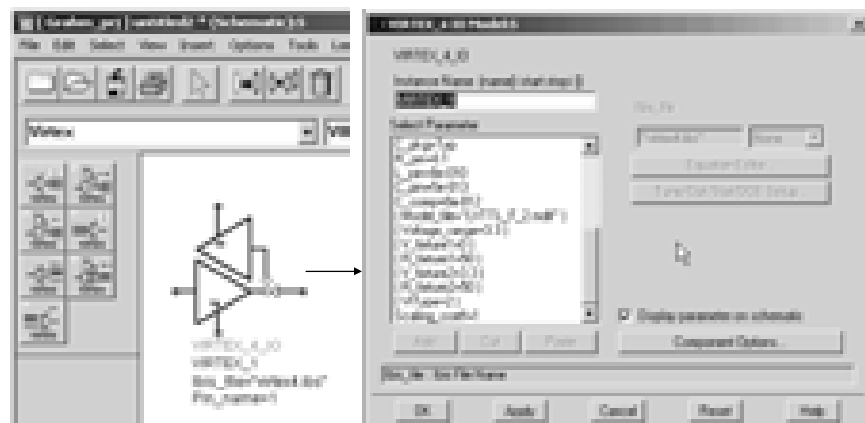


Page 81

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Feb. 23, 2006

IBIS design kit components



Page 82

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Feb. 23, 2006

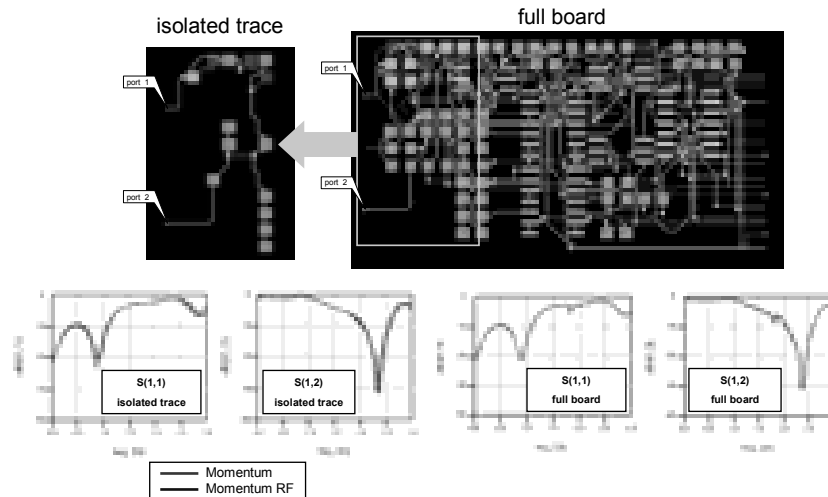
Using ADS for Signal Integrity Design Momentum

Page 85



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Feb. 23, 2006

Momentum RF for Digital Board Interconnect

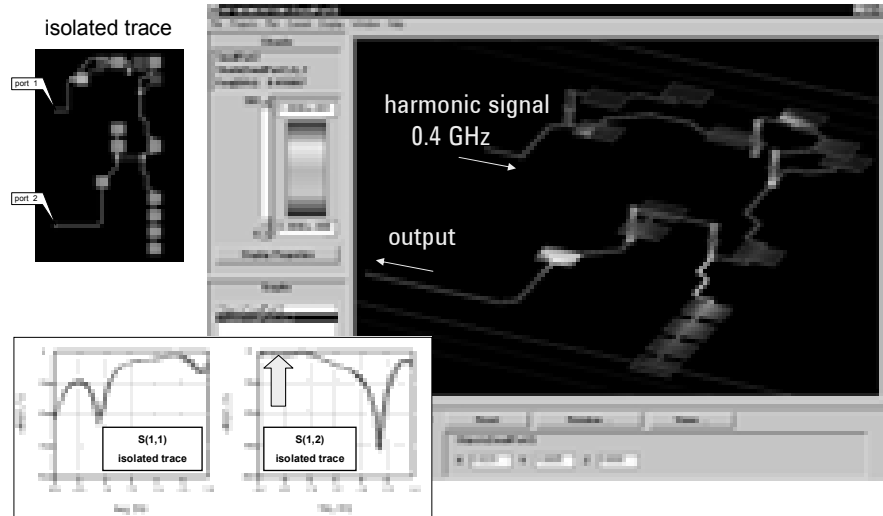


Page 86



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Feb. 23, 2006

Digital Board Interconnect - off resonance

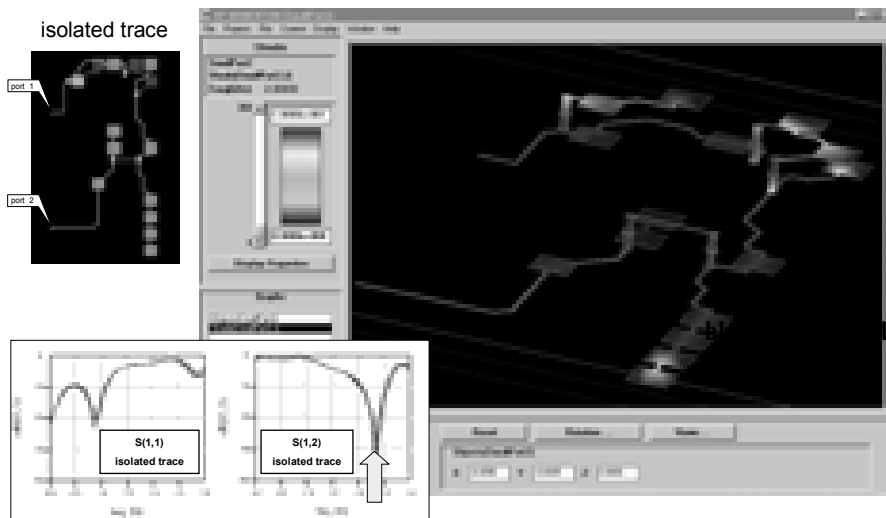


Page 87

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Feb. 23, 2006

Digital Board Interconnect - on resonance

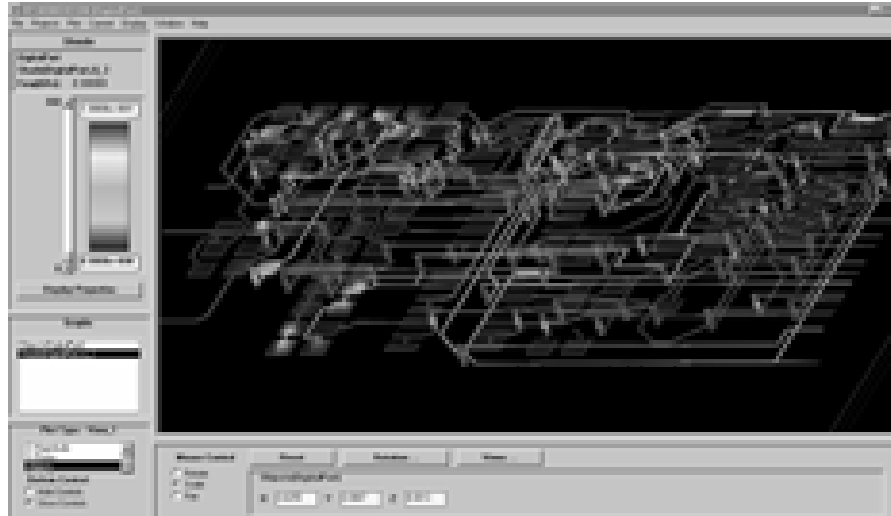


Page 88

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Feb. 23, 2006

Digital Board Interconnect

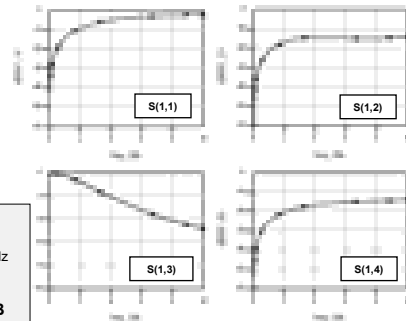
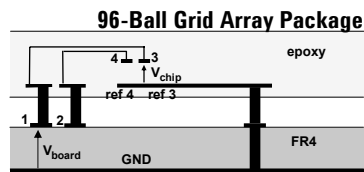
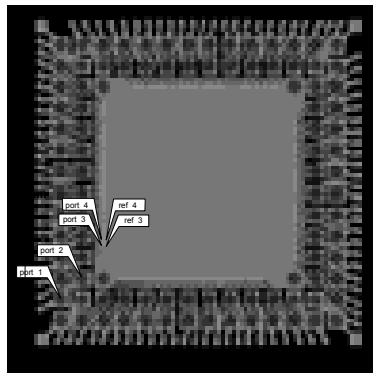


Page 89

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Momentum RF for Package Models



Momentum

Mesh: 20 cells/wavelength, 5 GHz

Matrix size : 8244
Process size : > 1 GB
User time : > 2 days

Momentum RF

Mesh: 20 cells/wavelength, 5 GHz

Matrix size : 1354
Process size : 106.57 MB
User time : 5h 17m 53s

PC-NT Pentium II workstation (330 MHz)

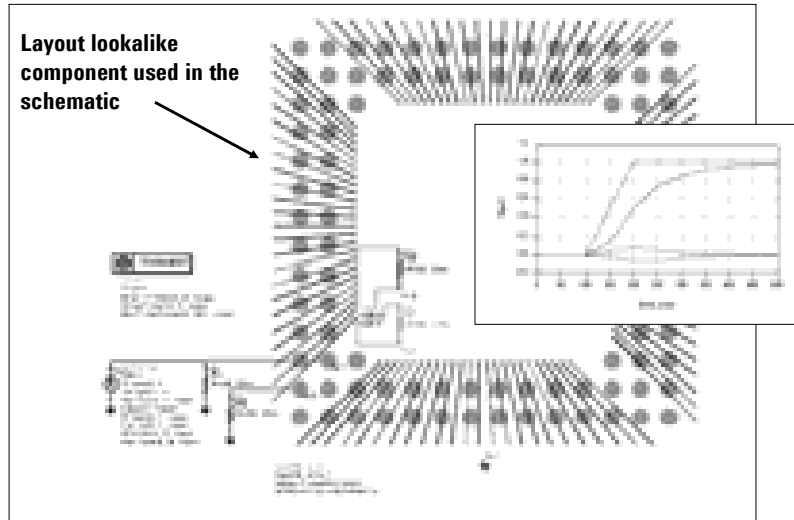
Rule of thumb: freq < 13.8 GHz

Page 90

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Feb. 23, 2006

Transient Simulation from Schematic



Page 91

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Feb. 23, 2006

Bringing it All Together

- ADS has been used for SI design for over 10 years
- ADS can act as a scalable design whiteboard
- ADS encourages you to be curious about your design ideas
- ADS has a multitude of accurate built-in models
- ADS allows you to build accurate physical models
- ADS lets you use your existing models
- ADS agrees with measurements
- ADS shows results the way you want to see them
- ADS brings IP, simulations and measurements together
- ADS Ptolemy lets you work with the whole Link before you build it!

Page 92

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Feb. 23, 2006

Advanced Calibration Techniques and Fixturing Issues for VNAs

Agilent Technologies Ltd.

Ming-Fan, Tsai
Application Engineer
Feb, 23, 2006

Page 1



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Feb. 23, 2006

Agenda

Overview of PNA FW Rev. 6.0

Application Code Version: A.06.00
Hard Disk Drive Version: S.05.40

Cal Registers

TRL Calibration with 4-port 20 GHz PNA-L

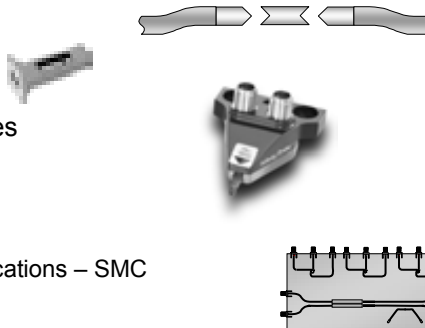
Unknown Thru Calibration

Offset Load Cal

Fixture And Probe Techniques

- Auto port extensions
- Embedding/de-embedding
- Frequency Converter Applications – SMC
- Measuring fixtures/probes

Q&A



Page 2



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Introduction - Goals and Objectives

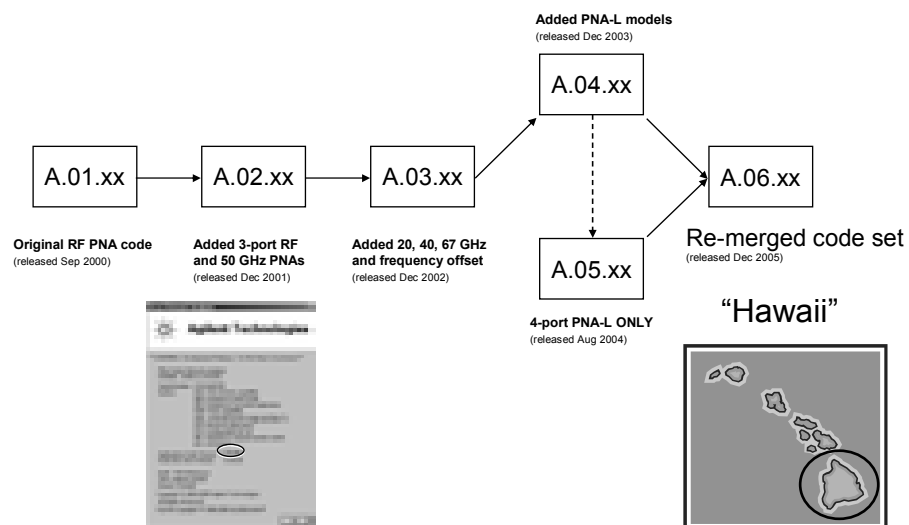
Course Goal

- Understand new calibration paradigm and features of PNA
- Get hands-on time on analyzer

Objectives

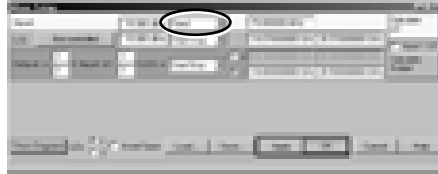
- Upon completion of this course you will be able to:
 - Calibrate a PNA and save a user cal set
 - Explain concept of Unknown Thru cal
 - Understand how a two-tier TRL cal is done
 - Recommend best cal approach for fixtured measurements

Welcome to PNA Firmware Revision A.06.0x



What's Totally New in 6.0...

- Target release date: 12 December, 2005
- Features
 - Calibrate using external trigger (e.g., during wideband pulse detection)
 - Calibrate with offset loads
 - External test set control
 - New FCA capability
 - file embedding during cal (for wafer probes and fixtures)
 - fixed input for up converters
 - 1.1 GHz CPU and related capabilities
 - Agilent VEE Runtime installed



What's New in 6.0 From 5.0...

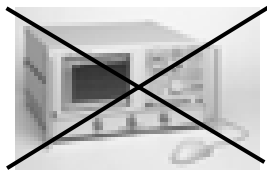
Note: Highlighted text describes features that are new for 2-port PNA/PNA-L models. These features have already been released for 4-port PNA-L models.

★ covered in this module

- | | |
|---|---|
| <ul style="list-style-type: none"> ★ TRL calibration for 4-port PNA-L <ul style="list-style-type: none"> Dedicated calibration window Calibration class label Data-based cal kits can now be modified Guided SmartCal supports ECal modules Option H11 verification Safely shutdown the PNA without a mouse ★ New *.csa save/recall file type <ul style="list-style-type: none"> 4-port fixture simulator functions <ul style="list-style-type: none"> • 4-Port network embed/de-embed • Balanced conversion • Differential-/ common-mode port Z conversion • Differential matching circuit embedding ★ Automatic port extensions <ul style="list-style-type: none"> Interface control Agilent 5091A test set control 8 traces per window (previously 4) | <ul style="list-style-type: none"> ★ CA on status bar <ul style="list-style-type: none"> .pdf version of Help file available New 4-port PNA Models: <ul style="list-style-type: none"> • N5230A Options 240 and 245 • Balanced measurements ★ Calibration registers <ul style="list-style-type: none"> Number of user ranges expanded to 16 (Stats and Markers) ★ Port extension toolbar features <ul style="list-style-type: none"> Magnitude offset ★ 2-port fixture compensation <ul style="list-style-type: none"> Two LO sources for millimeter-wave measurements Material handler trigger control Global pass / fail dialog Revised operator's check Revised system verification Guided calibration COM interface ★ Receiver power cal saved with cal set |
|---|---|

Will A.06.xx Work on Discontinued PNAs?

- ☒ "T1" RF PNA's (E8356/7/8A): Yes, with upgrade to Windows XP
- ☒ "T2" 2-port (E8801/2/3A): Yes, with upgrade to Windows XP
- ☒ "T2" 3-port (N3381/2/3A): No
- ☒ "M1" (E8364A): Yes, with upgrade to Windows XP
- ☒ XP upgrade: Order new disk drive from Agilent



What's New for the ENA

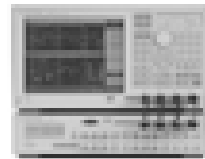
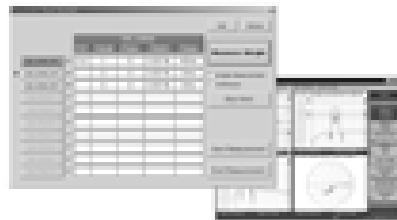
Rev 6.0 released 11/1/05

New features

- TRL/LRM & waveguide calibration
- Automatic port extensions
- 20,001 measurement points
- Complex reference impedance for balanced matching
- Flexible marker value display function
- User preset
- User recovery
- 13/16-port configurable test set control function

More info at:

[kobemktg.jp.agilent.com/field_eng/product/ena/customer_viewable/index.htm](http://kobemktg.jp/agilent.com/field_eng/product/ena/customer_viewable/index.htm)



Agenda

Overview of PNA FW Rev. 6.0

Application Code Version: A.06.00
Hard Disk Drive Version: S.05.40

➡ Cal Registers

TRL Calibration with 4-port 20 GHz PNA-L

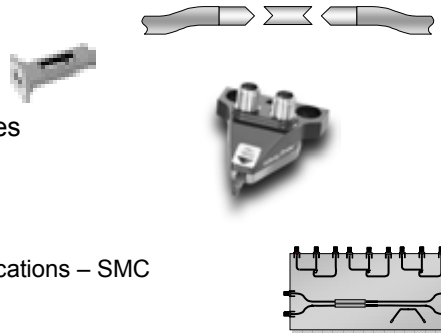
Unknown Thru Calibration

Offset Load Cal

Fixture And Probe Techniques

- Auto port extensions
- Embedding/de-embedding
- Frequency Converter Applications – SMC
- Measuring fixtures/probes

Q&A

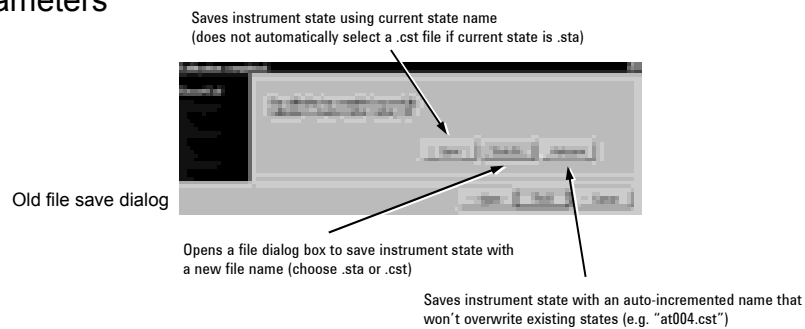


Old Calibration Paradigm

All calibrations were saved in a “calibration set”

“.cst” file pointed to data in a calibration set, but did NOT contain calibration data itself

“.cal” files contained calibration data but NOT instrument parameters



New Calibration Paradigm

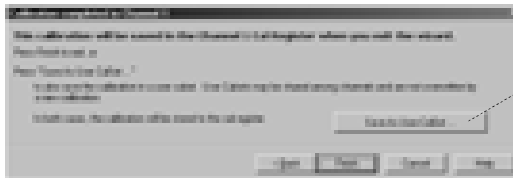
Cal Registers

- Each channel has its own cal register
- All cal data is saved to the channel cal register
- Data in cal register is “temporary” – data is saved on hard drive, BUT will be overwritten by the next calibration in that channel



User Cal Sets

- Old “Cal Sets” are now called “User Cal Sets”
- User must manually save data to a User Cal Set
- User cal sets are stored on the hard drive as before

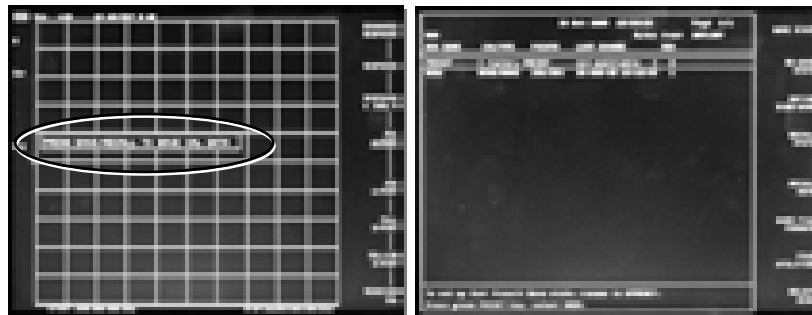


You no longer have a choice to save an instrument state!

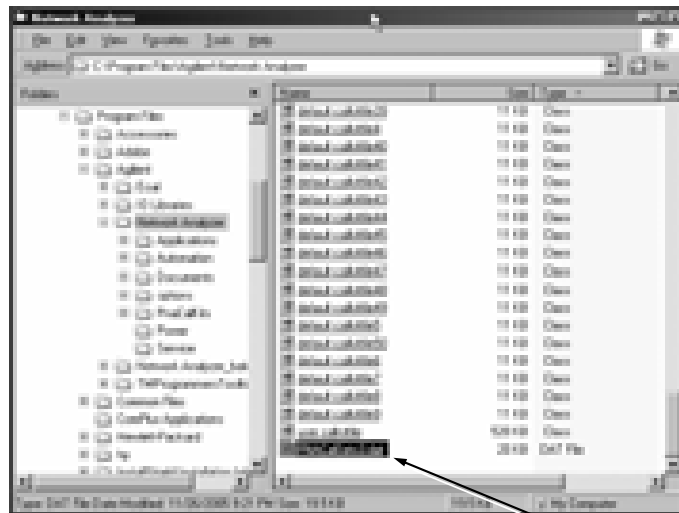
Cal Registers Should Be Familiar...

Cal register model is similar to that used in 8720s and 8510s

Cal registers prevent accumulation of unneeded cal sets

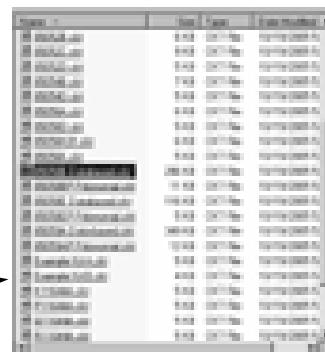
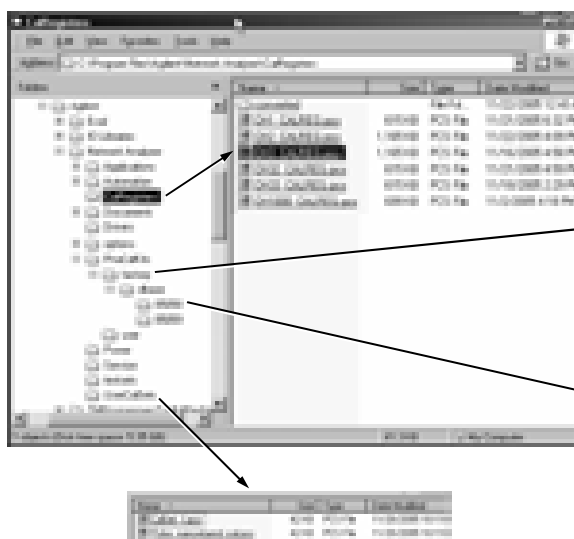


Old Calset File Location



All calset data was contained in this file

New Cal File Locations



Saving Instrument States and Cal Data

***.cst** - save instrument state and reference pointer to the cal set data

- data could be in cal register (not recommended)
- data could be in a user cal set (recommended)

New!

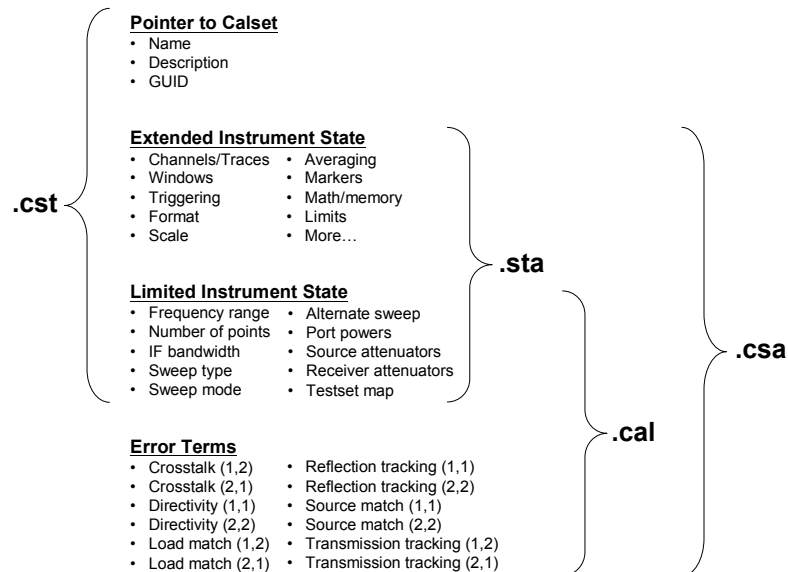
***.csa** - save instrument state and actual cal data (cal/state archive)

***.sta** - save instrument state ONLY (no calibration data)

***.cal** - save actual calibration data ONLY (no instrument state)



Instrument States and Cal Data



Receiver calibration

Receiver calibration gives corrected absolute power reading (for unratioed traces as opposed to an S-parameter traces)

Often used with FOM for measurements like harmonics, TOI

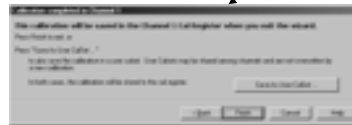
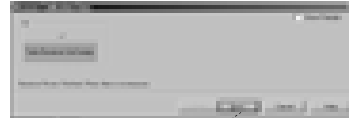
Uses power-meter-corrected internal source as a reference (source power cal)

Now saved as a cal set 

Multiple receiver cals requires separate channels for each cal

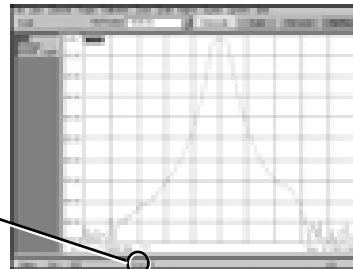
Source power calibrations

- No change from current behavior
- Saved as part of instrument states
- Not saved in cal sets



Correction Indicator on Status Bar

Symbol	Correction level	Accuracy
C	Full	Highest
C*	Interpolated	Uncertain
CA	Changed	Uncertain
No Cor	No correction	Lowest



C - Full correction

"C" is displayed immediately after a calibration is performed or when a valid Cal Set is applied. If you require optimum accuracy, avoid adjusting the analyzer's settings after calibration.

C* - Interpolated correction

"C*" appears in the status bar when interpolation is used during a measurement.

CA - Changed settings

"CA" appears in the status bar when one or more of the following stimulus settings change. The resulting measurement accuracy depends on which parameter has changed and how much it has changed. For optimum accuracy, recalibrate using the new settings.

- Sweep time
- IF bandwidth
- Port power
- Stepped sweep enabled/disabled

Agenda

Overview of PNA FW Rev. 6.0

Application Code Version: A.06.00
Hard Disk Drive Version: S.05.40

Cal Registers

➡ TRL Calibration with 4-port 20 GHz PNA-L

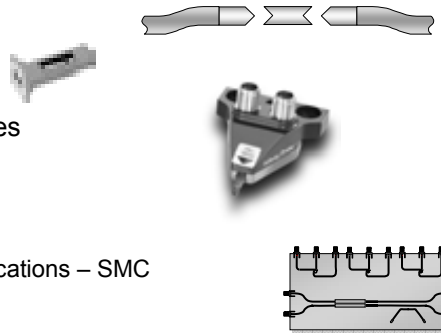
Unknown Thru Calibration

Offset Load Cal

Fixture And Probe Techniques

- Auto port extensions
- Embedding/de-embedding
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- Measuring fixtures/probes

Q&A



Page 19



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Feb. 23, 2006

TRL Calibration with 4-port 20 GHz PNA-L's

Yes, it can be done! (requires firmware A.05.25 and later)

Is “true” TRL calibration, not an approximation like TRL*

Two-step (two-tier) calibration process:

- Step 1: “Delta Match” calibration
- Step 2: Normal TRL calibration

What is a “Delta Match” cal?

- characterizes the difference (delta) between the source match and load match of each port of the VNA
- allows a VNA having a single reference receiver to perform TRL-style calibrations (including Unknown-Thru)



Page 20



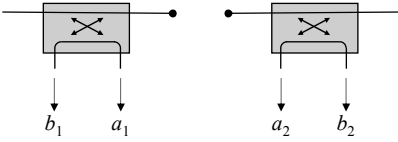
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Assumptions for TRL (and Unknown Thru)

8-term error model assume match at each test port remains constant, independent of whether it is a source or receiver

With real hardware, assumption is poor due to port switch

Generalized S-parameters for a two-port device:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{b_{11}}{a_{11}} & \frac{b_{12}}{a_{22}} \\ \frac{b_{21}}{a_{11}} & \frac{b_{22}}{a_{22}} \end{bmatrix}}_{\text{Ideal S-parameters}} \cdot \underbrace{\begin{bmatrix} 1 & \frac{a_{12}}{a_{22}} \\ \frac{a_{21}}{a_{11}} & 1 \end{bmatrix}}_{\text{Switch correction}}^{-1}$$


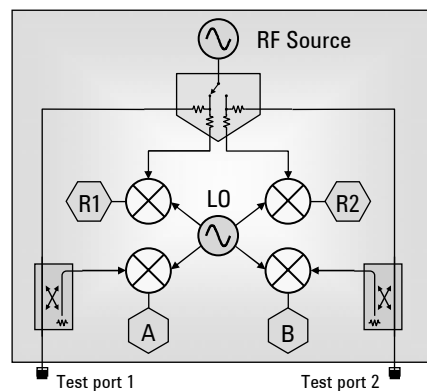
Note: $a_{11} = a_1^f$; $a_{12} = a_1^r$
 $a_{21} = a_2^f$; $a_{22} = a_2^r$

Two-Port Four-Receiver VNAs (like PNA)

Dual reflectometers replaced by splitters and 3-port couplers

Incident wave detection is still after the port switch

Switch corrections a_{12}/a_{22} and a_{21}/a_{11} can be directly measured

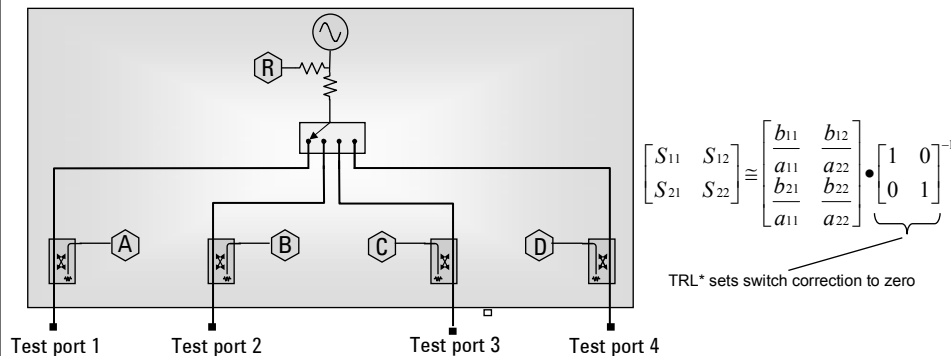


Single Reference Receiver VNAs (like 4-Port PNA-L)

Reference receiver is prior to port switch

Switch corrections cannot be directly measured

TRL* ignores switch correction terms by setting them to zero



Page 23

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Feb. 23, 2006

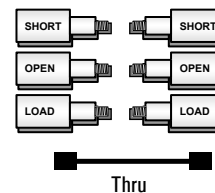
Alternative to Measuring Switch Corrections

Instead of ignoring the switching terms, we can characterize the match differences and then apply them during the TRL cal

To do so, we can restate the switch correction terms:

$$\begin{bmatrix} 1 & \frac{a_{12}}{a_{22}} \\ \frac{a_{21}}{a_{11}} & 1 \end{bmatrix}^{-1} = \begin{bmatrix} 1 & \frac{b_{12} a_{12}}{a_{22} b_{12}} \\ \frac{b_{21} a_{21}}{a_{11} b_{21}} & 1 \end{bmatrix}^{-1} = \begin{bmatrix} 1 & \frac{b_{12}}{a_{22}} \Gamma_r \\ \frac{b_{21}}{a_{11}} \Gamma_f & 1 \end{bmatrix}^{-1}$$

Γ_f and Γ_r are “delta-match” terms, and they can be derived from an SOLT calibration



Page 24

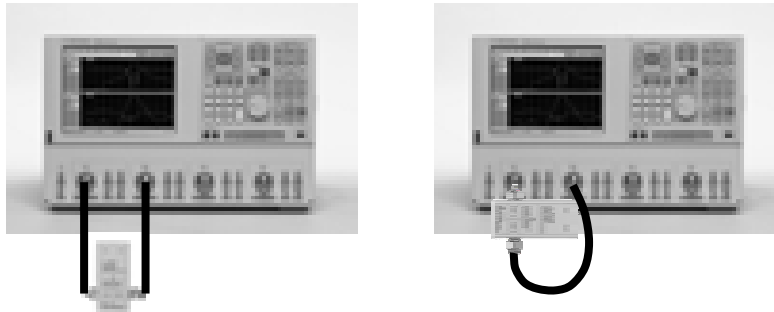
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Delta Match Cal

Delta match cal characterizes internal match differences, so it can be performed...

- with mixed connector types
- with or without test port cables, in any combination
- with adapters that can remain or be removed for subsequent TRL cals



When is Delta Match Used?

Cal Method	Uses Delta Match?
SOLT - Known Thru (Includes Flush-Thru, Known-Thru and Minimized Thru)	No
SOLT - Adapter Removal	No
SOLT - Unknown Thru	Yes
TRL - Known Thru	Yes
TRL - Adapter Removal	Yes
ECal Internal Thru	No
ECal Unknown Thru	Yes

Definitions

- Flush thru: insertable, zero-length
- Known thru: characterized (all 4 S-parameters)
- Unknown thru: reciprocal ($S_{21}=S_{12}$); usually low-loss and well matched

Two Ways to Perform the Delta-Match Calibration

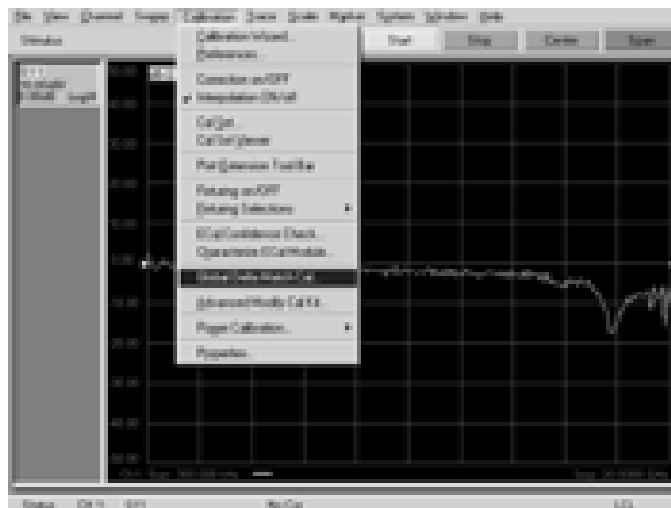
Global Delta Match

- Covers entire frequency range of instrument
- Interpolation used for TRL cals with smaller spans and/or less points
- Only one global delta match cal set can exist at a time
- Future: considering providing factory global delta match cal set

User Delta Match

- Perform a non-TRL calibration, such as mechanical SOLT, SOLR or ECal
- Save data as a normal user cal set
- Frequency range and number of points must be identical to that of the follow-on TRL calibration
- Interpolation is not used during the calibration, but can be used for measurements

Performing the Global Delta Match Cal

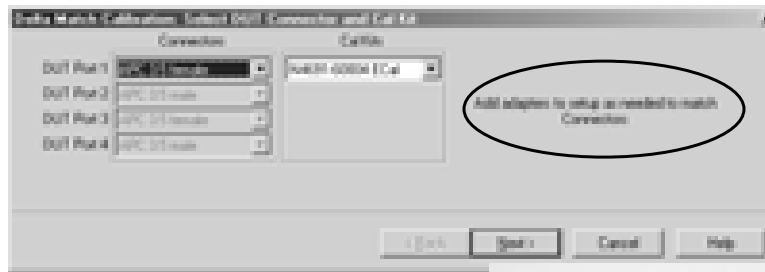


Default Settings:

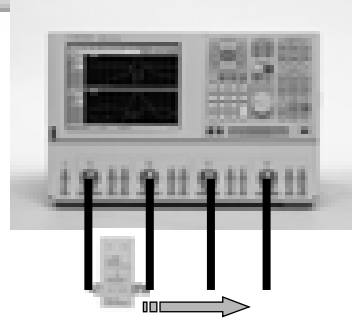
Points: 1601
IF BW: 100 Hz
Freq: 300 kHz -
20.1 GHz

User cannot change
these settings!

Performing the Global Delta Match Cal



- Select DUT connectors (the only choice you have is in choosing the “DUT Port 1” connector)
- Add adapters to match those shown in the table
- ECal provides the easiest solution, especially with the new 4-port 20 GHz module (N4432/3A)

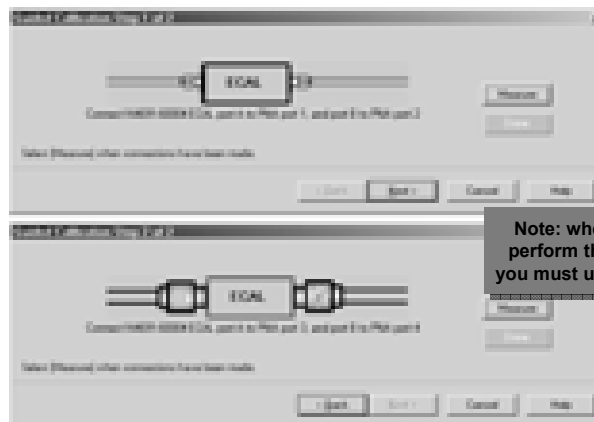


Page 29

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Using 2-Port ECal Modules



With a 2-port ECal, it only takes two steps to complete the cal!

Step 1 of 2: connect ECal to ports 1 and 2

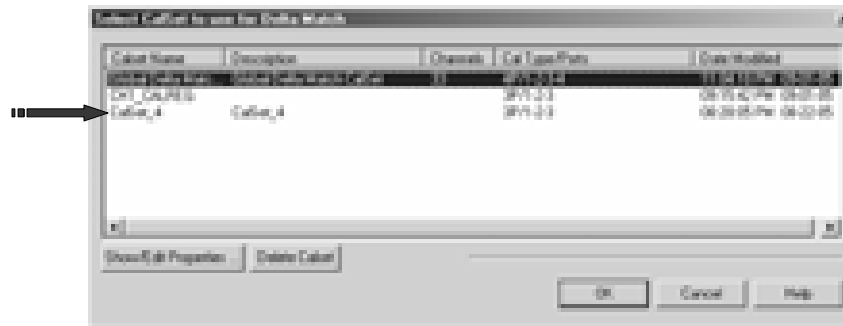
Step 2 of 2: connect ECal to ports 3 and 4

Page 30

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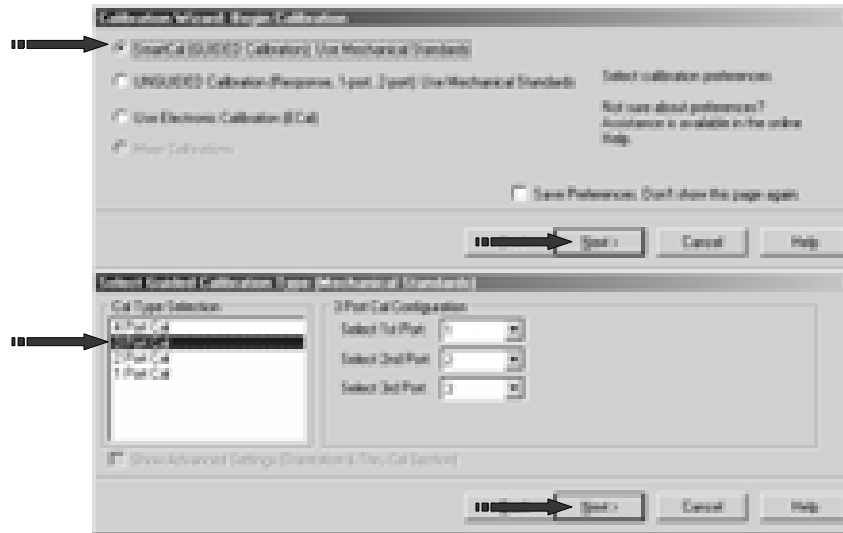
User Delta Match



Instead of selecting the Global Delta Match CalSet, select an available user CalSet that matches the current stimulus conditions

Performing the TRL Calibration

Calibration > Calibration Wizard

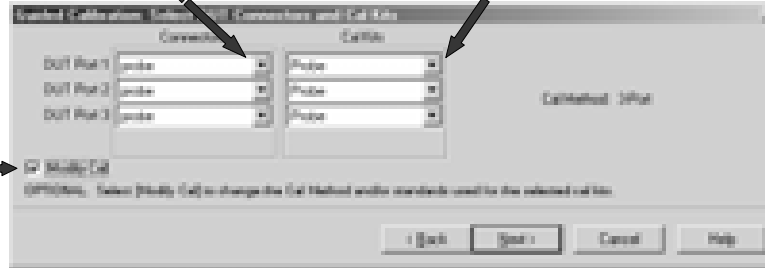


Performing the TRL Calibration

Use dropdown menu to select connectors.

Appropriate cal kits should appear based on connector type. Use dropdown menu to select Cal Kit.

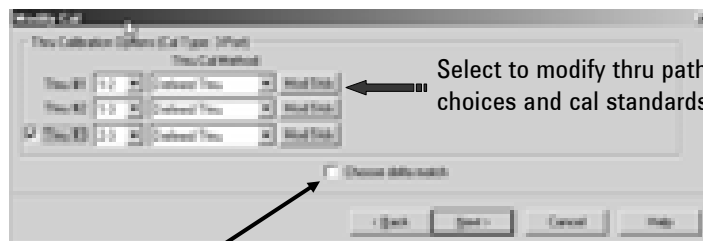
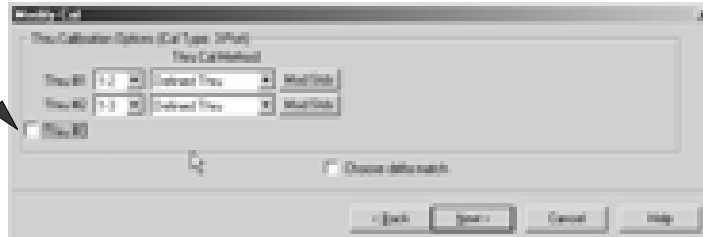
Select this and the following screen will appear. Otherwise, the default uses the existing Global Delta Match Cal.”



Here, as a test case, we created a cal kit definition using “probe” as connector type. In this cal kit, we defined Short, Thru and Line standards. Plus, we have given them TRL class assignments.

Performing the TRL Calibration

Default is “minimum thru’s” (known bug: TRL always measures all paths, regardless of the status of this box)



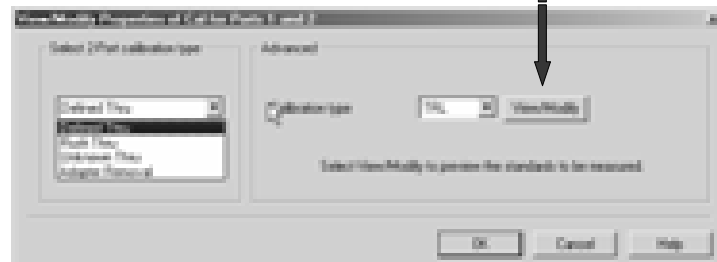
Select to modify thru path choices and cal standards.

Select this to choose the “delta match” calset.

Performing the TRL Calibration

- Selecting “Mod Stds” brings up this screen
- In this case, the default is TRL with Defined Thru
- If you select another thru choice, then cal type will be SOLT
- Generally, you do not need to select “View/Modify”

Click here to view class assignments



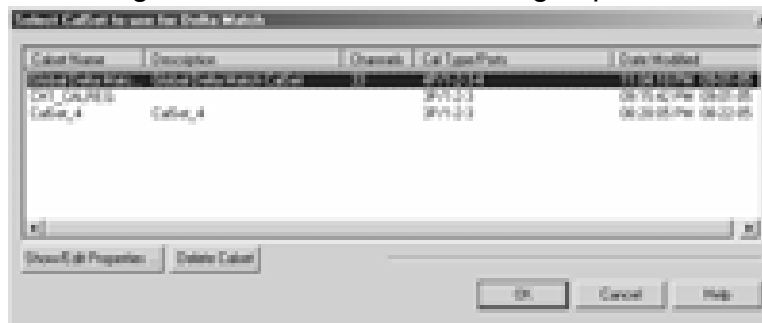
Page 35

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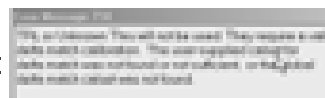
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Performing the TRL Calibration

Selecting “Choose Delta Match” brings up this screen



- All cal sets will appear, but not all will work for delta match
- Highlight the file you want and click OK
- If you pick a “bad” user cal set, you get this error:



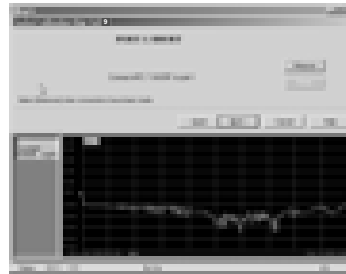
Page 36

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Performing the TRL Calibration

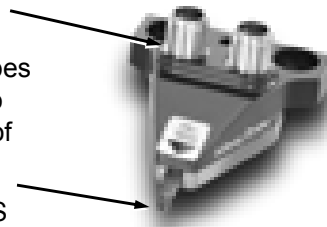
- At this point, the calibration should start.
- Based on the “probe” cal kit we created, we went through the following steps for a 3-port TRL cal:
 - Step 1 of 9, short to port 1
 - Step 2 of 9, short to port 2
 - Step 3 of 9, thru between ports 1 and 2
 - Step 4 of 9, line between ports 1 and 2
 - Step 5 of 9, short to port 3
 - Step 6 of 9, thru between ports 1 and 3
 - Step 7 of 9, line between ports 1 and 3
 - Step 8 of 9, thru between ports 2 and 3
 - Step 9 of 9, line between ports 2 and 3



What About Calibrating On-Wafer?

Because delta-match cal can be performed at any interface, on-wafer customers have the following options:

- Use ECal (or mechanical cal kit) at the end of the cables, before connecting to the probes (probes tend to have female connectors, so simply add adapters to make up two pairs of insertable cals)
- Use the probes with a 4-port with SOLT ISS



Cascade's WinCal 2006

- Will not support 4-port TRL calibrations initially
- Allows advanced 2-port calibrations, such as the LRRM family

Frequently Asked Questions

Can I perform a 4-port TRL calibration?

-- **Yes**, simply follow the same steps covered in this presentation

Is TRL calibration limited to only 2 ports?

-- **No**, it can be used with 3- or 4-port calibrations as well

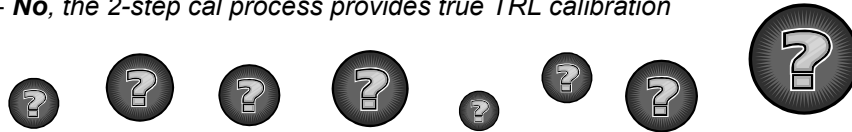
Can I perform a 4-port TRL calibration on-wafer? -- **Yes**

Since the 4-port 20 GHz PNA-L has only one reference receiver, do I need a hardware upgrade before I can perform a TRL calibration?

-- **No**, the 2-step calibration process does NOT require any hardware upgrade, but may require a firmware upgrade

Since the 4-port 20 GHz PNA-L has only one reference receiver, does this mean we can only do TRL*?

-- **No**, the 2-step cal process provides true TRL calibration



TRL Summary

PNA's & 2-port PNA-L's with dedicated two reference receivers (incident wave detectors occur after the switch)	TRL – directly measure “switch correction” terms
Legacy 872x family with one reference receiver (switch occurs after the incident wave detector)	TRL* – ignore “switch correction” terms
4-port 20 GHz PNA-L with one reference receiver (switch occurs after the incident wave detector)	TRL – first characterize the match differences with delta match cal and then use them during TRL calibration

New application note:

On-Wafer Calibration Using a 4-Port 20 GHz PNA-L, **5989-2287EN**

Agenda

Overview of PNA FW Rev. 6.0

Application Code Version: A.06.00
Hard Disk Drive Version: S.05.40

Cal Registers

TRL Calibration with 4-port 20 GHz PNA-L

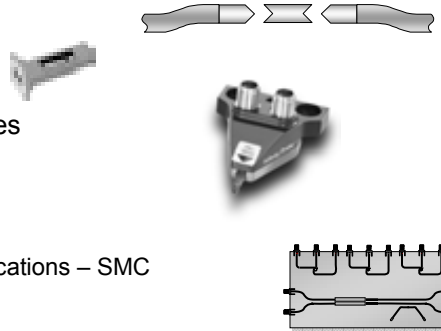
➡ Unknown Thru Calibration

Offset Load Cal

Fixture And Probe Techniques

- Auto port extensions
- Embedding/de-embedding
- Frequency Converter Applications – SMC
- Measuring fixtures/probes

Q&A



Unknown Thru – Agilent's ~~Secret~~ Weapon!

“Unknown Thru” (aka SOLR) algorithm is useful for both insertable and non-insertable calibrations

Traditional non-insertable methods:

- Swap equal adapters
- Use characterized thru (S-parameters known)
- Perform adapter removal cal
- Add adapters after cal, then, during measurement...
 - use port extensions
 - de-embed adapters (S-parameters known)



Compromises of Traditional Methods

Swap equal adapters

- Need phase matched adapters of different sexes (e.g., f-f, m-f)
- Error results from loss and mismatch differences of adapters

Use characterized thru

- Multi-step process
- Need a non-insertable cal to measure S-parameters of characterized thru

Perform adapter removal cal

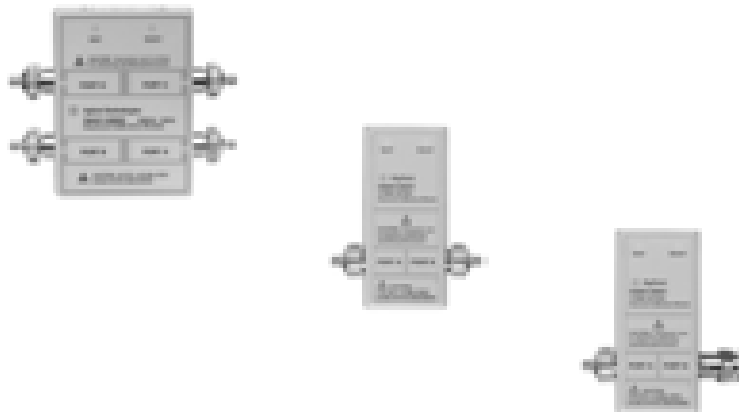
- Accurate but many steps in calibration (two 2-port calibrations)

Add adapters after cal, then, during measurement...

- Use port extensions – doesn't remove adapter mismatch effects
- De-embed adapters (S-parameters known) – similar to characterized thru

Non-Insertable ECal Modules

ECal resolves many, but not all non-insertable situations



Unknown Thru to the Rescue!

Unknown Thru calibration makes 2-port calibrations much easier!

No need for matched or characterized thru adapters!

Works great for

- Non-insertable calibrations



- Fixed port positions



- Physically loooooooooong DUTs



- Port orientations that are not in-line



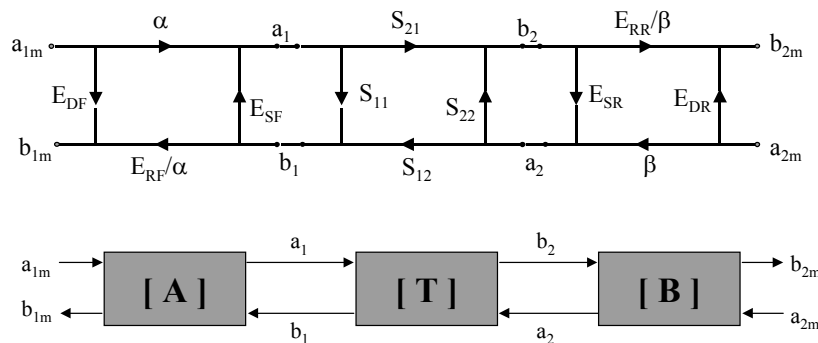
- Multiport devices



Note: Unknown Thru only works with guided calibrations

Unknown Thru Algorithm

Unknown thru algorithm uses "TRL" 8-term error model



Unknown Thru Calibration Requirements

Systematic errors of all test ports (directivity, source match, reflection tracking) can be completely characterized

“Unknown thru” calibration standard:

- Must be reciprocal ($S_{ij} = S_{ji}$)
- Phase known to within a quarter wavelength

VNA signal-path switch errors can be quantified

- Requires dual reflectometers on all ports
(e.g., a 2-port 4-receiver VNA) OR
- Requires delta-match correction

Two-Port Unknown Thru Calibration Sequence

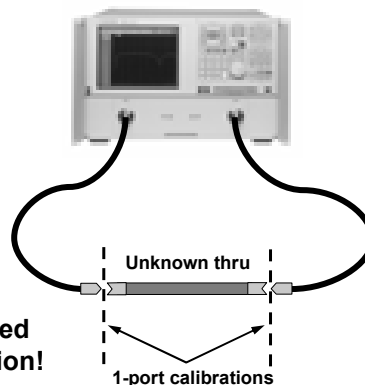
Measure open, short, load on port 1

Measure open, short, load on port 2

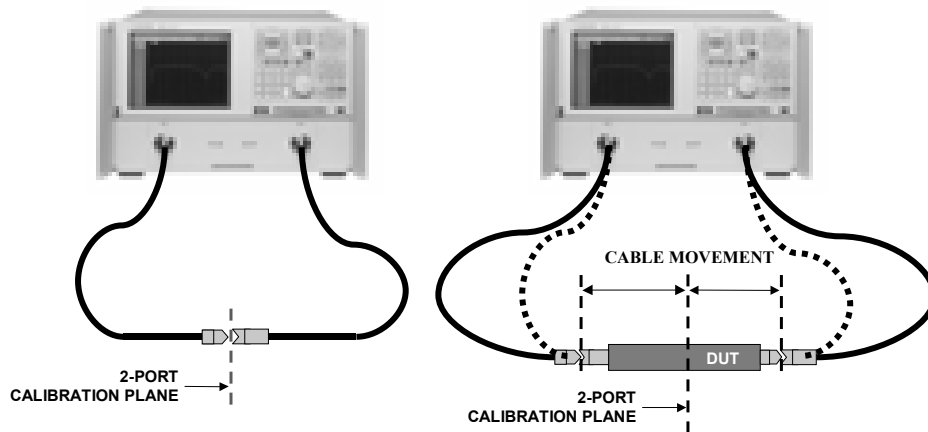
Measure insertable adapter (unknown thru)
between ports 1 and 2

Confirm estimated electrical
delay of unknown thru

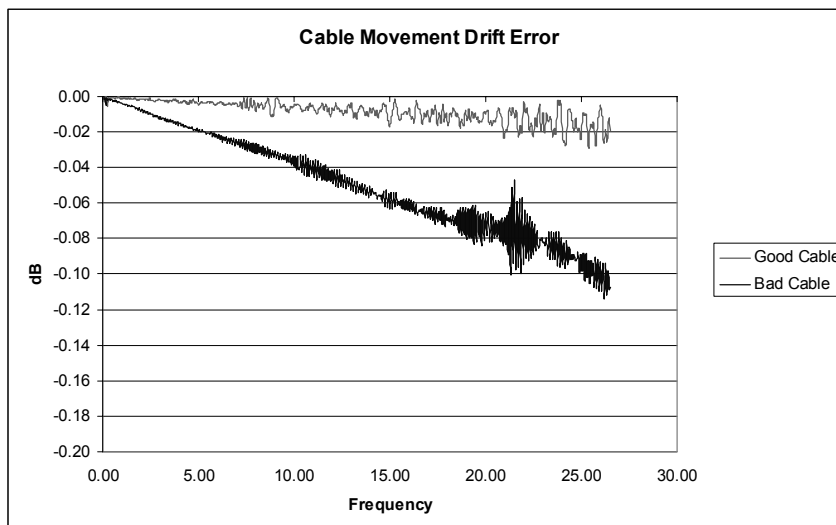
Unknown Thru calibration is performed
just like a “flush thru” 2-port calibration!



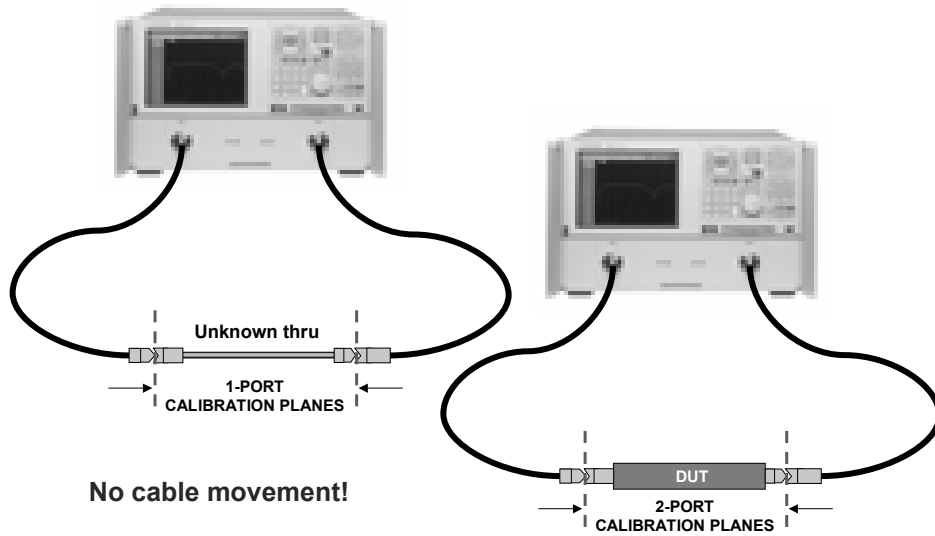
Measuring Physically Long Devices (Usual Way)



Cable Movement Error



Measuring Physically Long Devices (Unknown Thru)

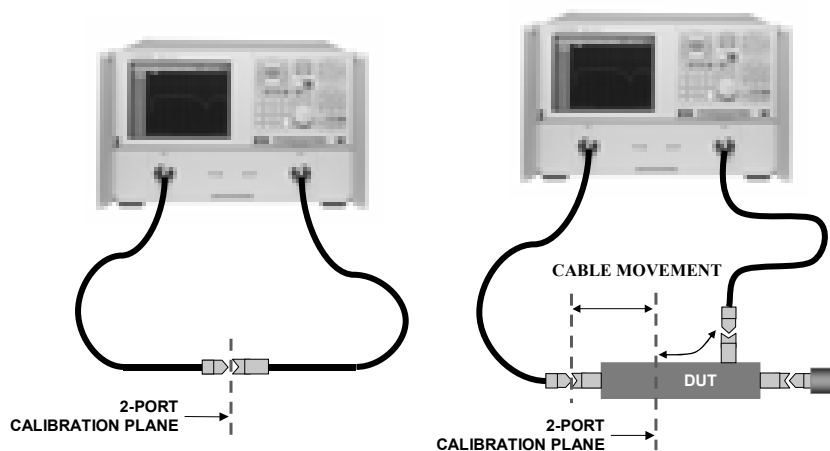


Page 51

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Measuring Devices with Non-Aligned Ports (Usual Way)

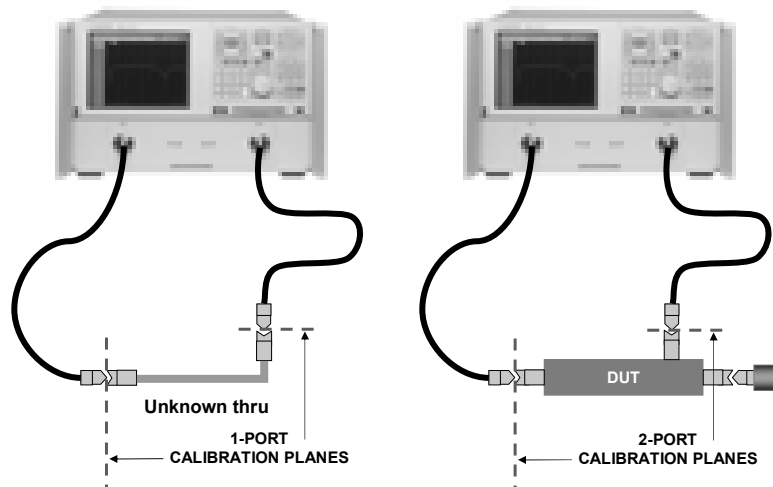


Page 52

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Measuring Devices with Non-Aligned Ports (Unknown Thru)

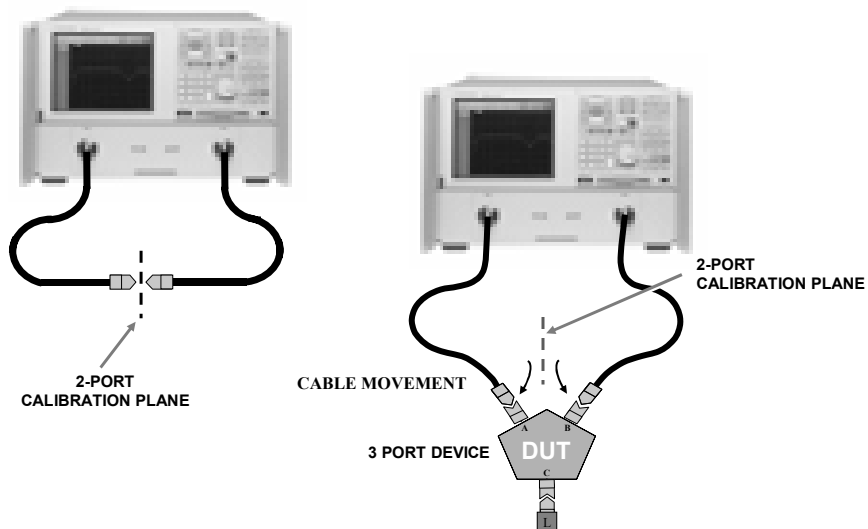


Page 53

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Multiport and Non-Aligned Case (Usual Way)

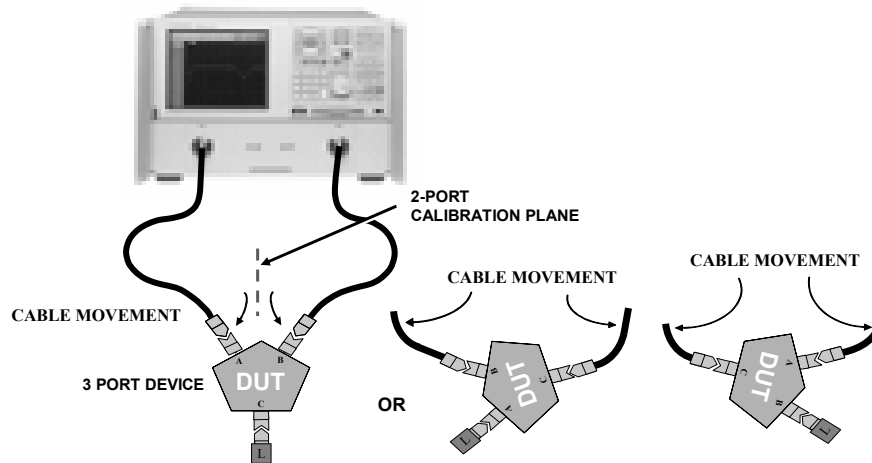


Page 54

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Multiport and Non-Aligned Case (Usual Way)

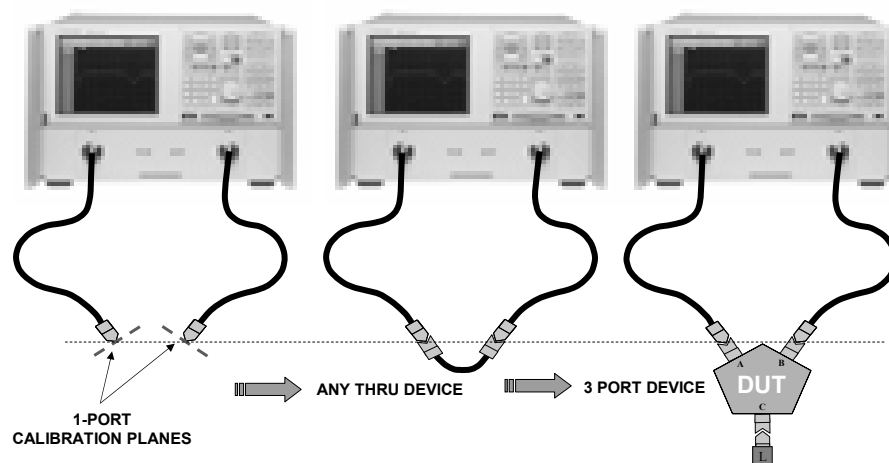


Page 55

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Multiport and Non-Aligned Case (Unknown Thru)

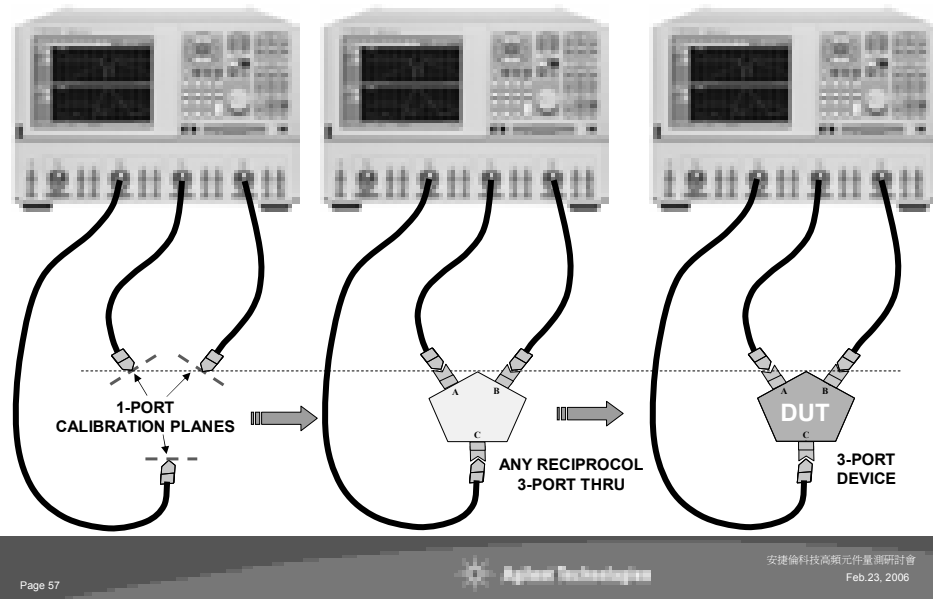


Page 56

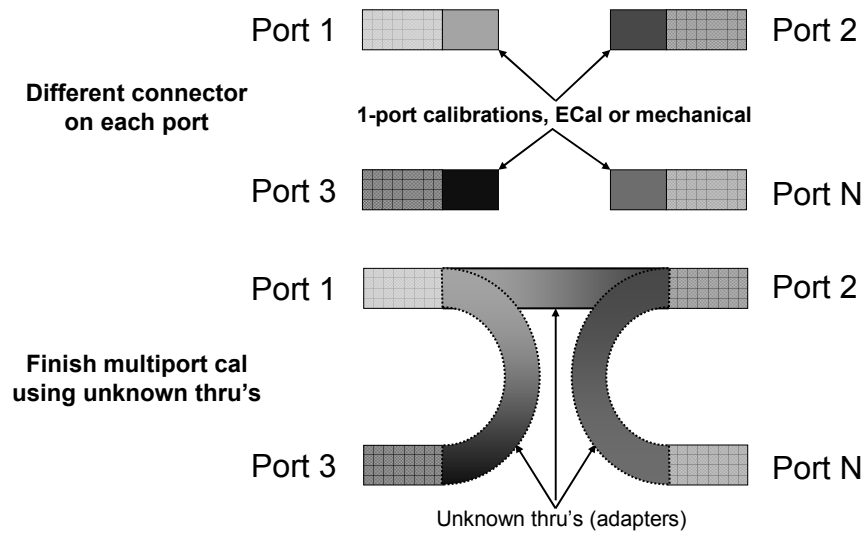
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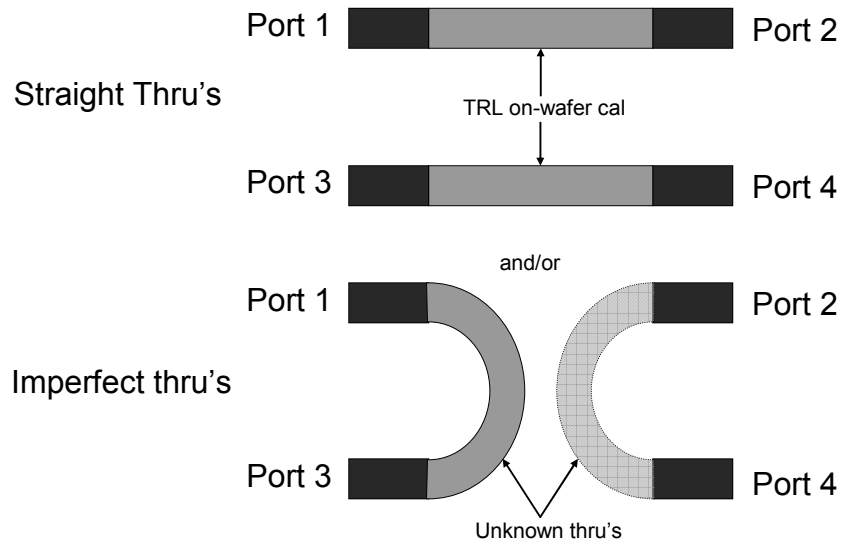
Multiport and Non-Aligned Case (Unknown Thru)



Multiport Unknown Thru with Different Connectors



On-Wafer Calibrations Using Unknown Thru's

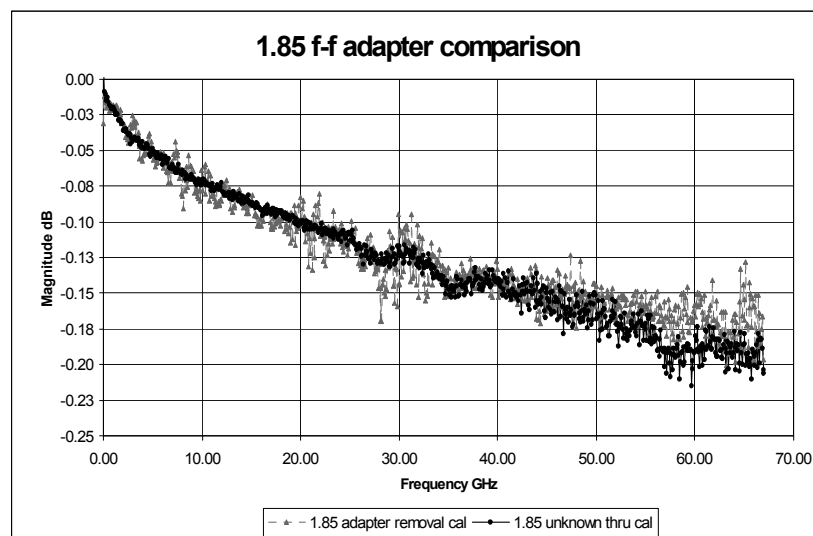


Page 59

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Unknown Thru and Adapter Removal Compared



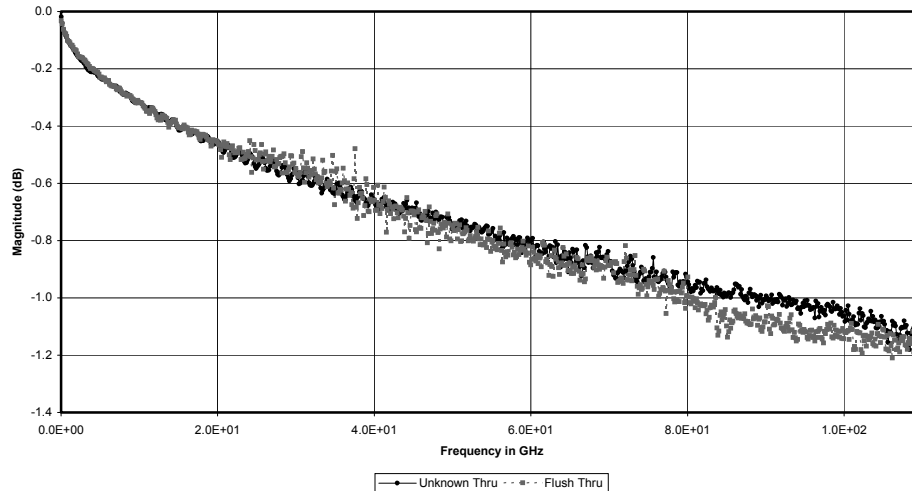
Page 60

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Unknown Thru and Flush Thru Compared

Long (Aspect Ratio) Device, 3.5 inch x 1 mm cable, Test Comparison



Page 61

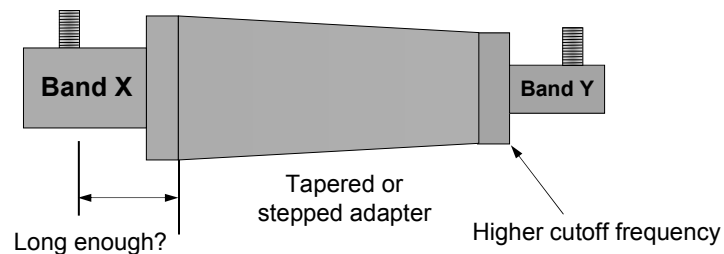
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Unknown Thru For Different Waveguide Bands

Watch out for these potential problems:

1. Non-overlapping waveguide bands
2. Attenuation near cutoff may be too high for thru calibration
3. Higher-order modes
(longer adapters better attenuate undesired modes)



Page 62

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Known Thru Versus Unknown Thru

Known Thru	Unknown Thru
Requires data or model and VERY stable device	Requires S21=S12
Can not use any device	Any passive device OK
Accuracy sensitive to E_D , E_S , S-parameter errors and thru S21	Accuracy sensitive to E_S and E_R errors
S-parameters can change	NA
Characterization error sensitive to cable movement stability	NA
Requires periodic calibration	NA
Can not tolerate bad connection	Bad connection not a problem

Agenda

Overview of PNA FW Rev. 6.0

Application Code Version: A.06.00
Hard Disk Drive Version: S.05.40

Cal Registers

TRL Calibration with 4-port 20 GHz PNA-L

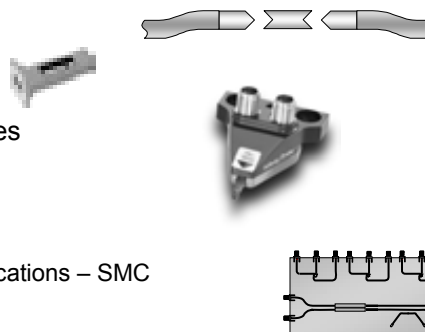
Unknown Thru Calibration

➡ Offset Load Cal

Fixture And Probe Techniques

- Auto port extensions
- Embedding/de-embedding
- Frequency Converter Applications – SMC
- Measuring fixtures/probes

Q&A



Offset Load Calibration Overview

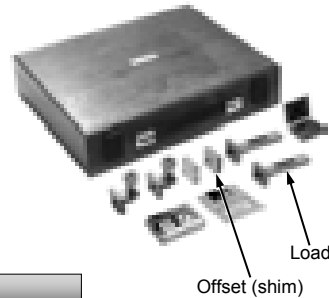
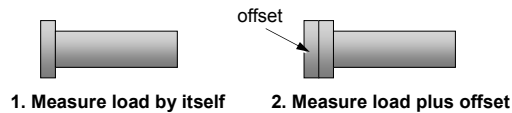
Offset load calibration originated with 8510

Offset load is a compound standard – load is connected multiple times with differing offsets

In simplest and most common form, there are just two connections: the load by itself, and the load with an offset

Similar to a sliding load standard, except offsets are set by a known, precise transmission line (e.g., a waveguide section)

Not the same as a load standard with defined delay, which is a single standard



Page 65

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Offset Load Calibration Advantages

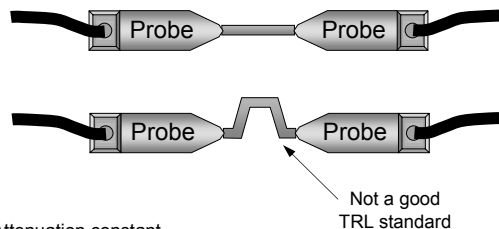
Provides higher directivity and load match accuracy when the definition of the offset is better known than the load definition

Does not require a dual reflectometer VNA as it uses SOLT error model instead of TRL error model

Ideal for 1-port calibrations

Also helpful in situations where calibration planes cannot physically move, such as fixed probe or waveguide positions, where TRL calibrations are difficult

Offset standard can include loss term (especially valuable near cutoff frequency)



Page 66

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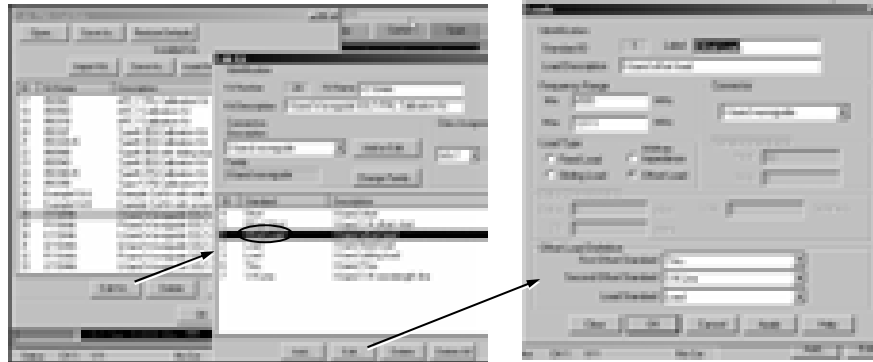
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Offset Load Definition

Only available in guided calibration (SmartCal)

Math is enhanced over what 8510 did

New FW added offset load standards to waveguide cal kits



Page 67

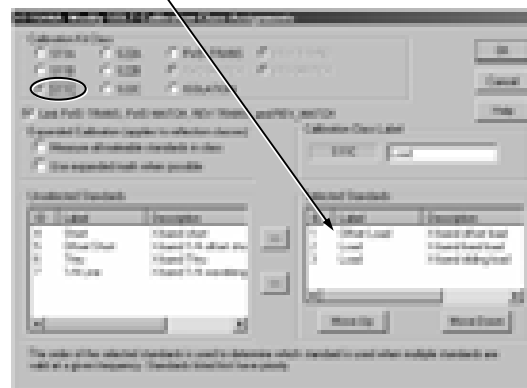
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Offset Load Class Assignments

SmartCal uses as many standards as it needs to complete calibration, based on frequency range of standards

In this case, only offset load is used



Page 68

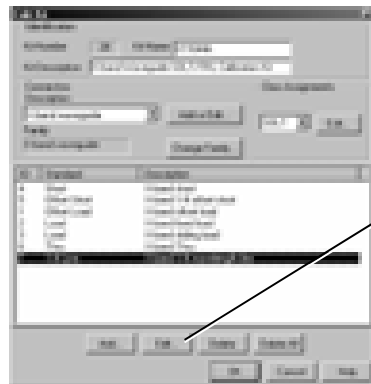
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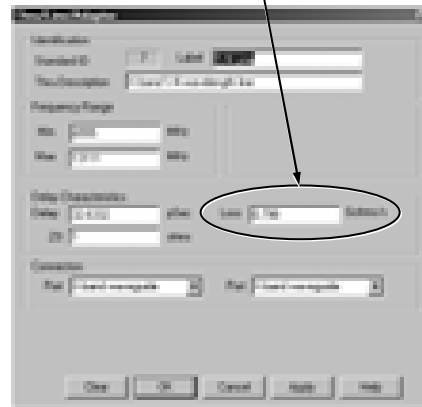
Thru Loss Definition

8510 did not use loss term

PNA includes loss for better accuracy, especially near cutoff and with poor raw source match



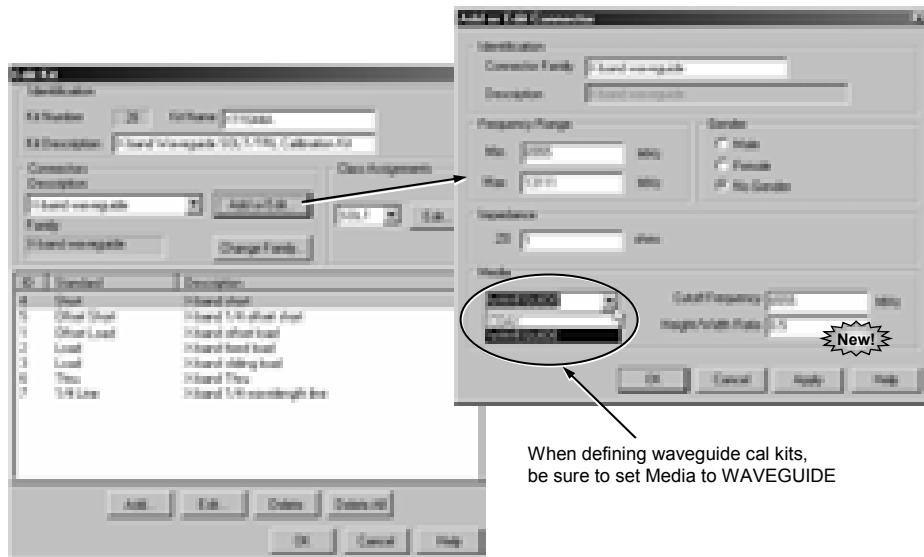
Enter waveguide loss here (different model than coaxial loss model)



$$\text{offset loss (waveguide)} = \frac{\sqrt{\pi \mu_0 f_c \rho}}{h} \times \left(\frac{v}{\sqrt{\epsilon_r}} \right)$$

μ_0 = free space permeability
 f_c = waveguide cut off frequency
 ρ = resistivity of waveguide metal
 h = waveguide height (short dimension)
 v = velocity of light
 ϵ_r = permittivity of dielectric (usually air)

Waveguide Connector Definition



When defining waveguide cal kits,
be sure to set Media to WAVEGUIDE

Agenda

Overview of PNA FW Rev. 6.0

Application Code Version: A.06.00
Hard Disk Drive Version: S.05.40

Cal Registers

TRL Calibration with 4-port 20 GHz PNA-L

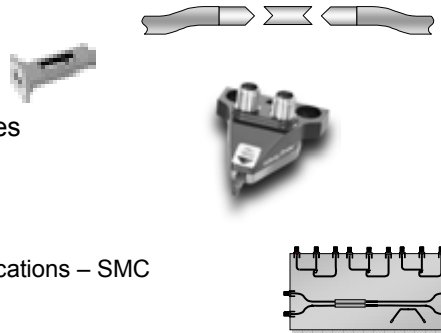
Unknown Thru Calibration

Offset Load Cal

➤ Fixture And Probe Techniques

- Auto port extensions
- Embedding/de-embedding
- Frequency Converter Applications – SMC
- Measuring fixtures/probes

Q&A

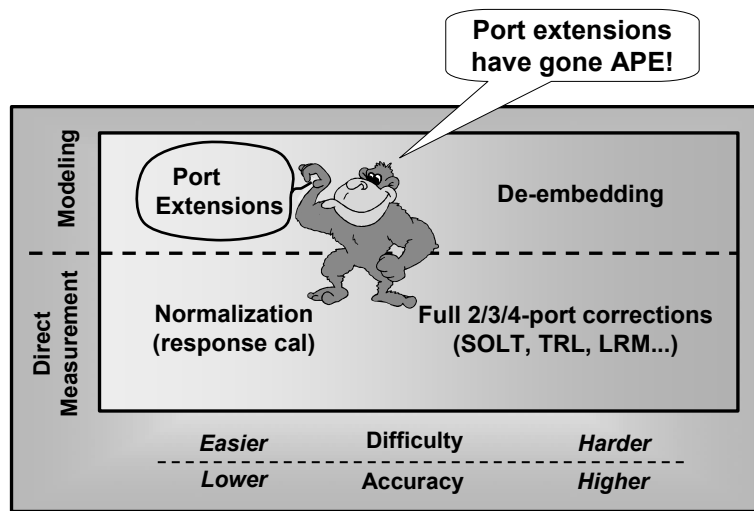


Page 71

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Error Correction Choices



Page 72

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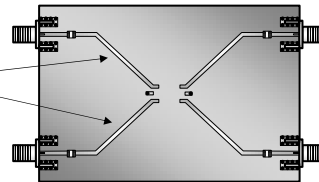
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APE = Automatic Port Extensions



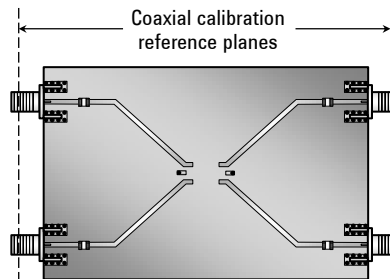
- First solution to apply both electrical delay and insertion loss to enhance port extensions
- First approach to give reasonable alternative to building in-fixture calibration standards or de-embedding fixture

APE accounts for loss and phase of fixture transmission lines



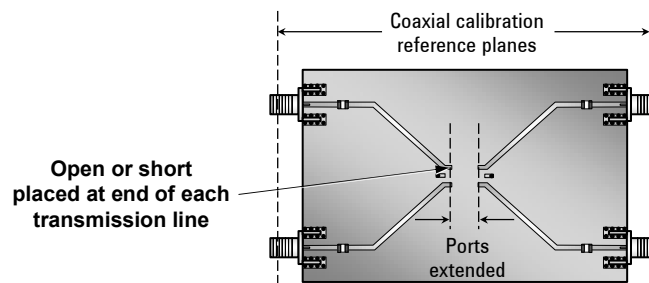
Automatic Port Extensions – Step 1

- First, perform coaxial calibration at fixture connectors to remove errors due to VNA and test cables
- At this point, only the fixture loss, delay and fixture mismatch remain as sources of error.



Automatic Port Extensions – Step 2

- After coaxial calibration, connect an open or short to portion of fixture being measured
- Perform APE: algorithm measures each portion of fixture and computes insertion loss and electrical delay
- Values calculated by APE are entered into port extension feature
- Now, only fixture mismatch remains as source of error (dominated by coaxial connector).



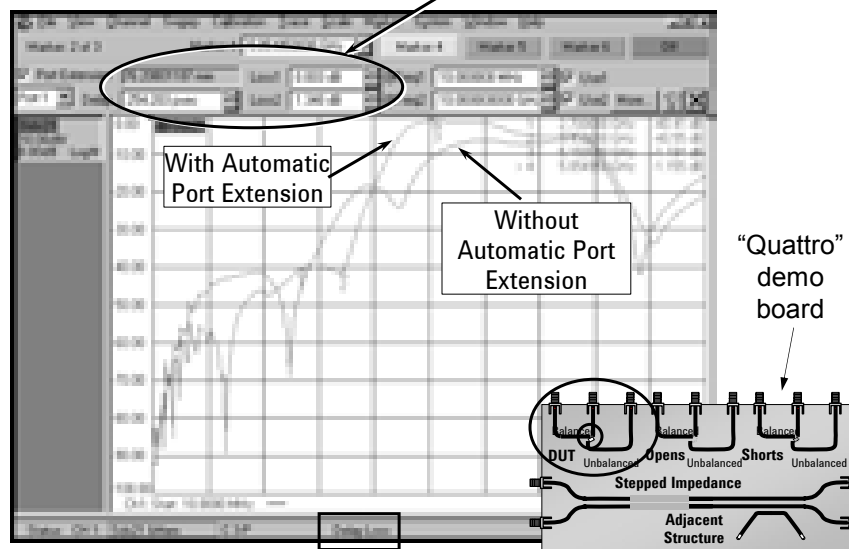
Page 75

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Feb. 23, 2006

Measurement Results

Delay & loss compensation
(values computed by APE)



Page 76

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Automatic Port Extension – Implementation

Measures S_{ii} (reflection) of each port

Uses ideal open or short models

Computes electrical delay using best-fit straight-line model

Computes insertion loss using a best-fit dielectric loss model

- Default setting uses frequencies in *Active Channel Stimulus* (results in loss at two frequencies)
- Active Marker choice uses frequency at *Active Marker* (results in loss at one frequency only)

Computed delay & loss values are automatically displayed via new port-extension tool bar

Values can be saved as part of instrument state or recorded for manual insertion next time

How is the Loss Term Calculated?

Loss is calculated for each frequency data point (f) as follows:

If Use1 is checked and NOT Use2 then:

- $\text{Loss}(f) = \text{Loss1} * (f/\text{Freq1})^{0.5}$ (coaxial loss model)

If Use1 AND Use2 are checked, then:

- $\text{Loss}(f) = \text{Loss1} * (f/\text{Freq1})^n$ (printed circuit board dielectric loss model)
- Where $n = \log_{10} [\text{abs}(\text{Loss1}/\text{Loss2})] / \log_{10} (\text{Freq1}/\text{Freq2})$

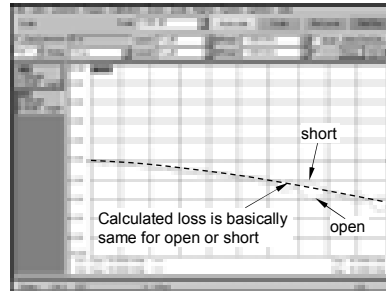


Which Standards Should I Use?

For broadband applications, shorts or opens work equally well
Choose the most convenient standard (often an open) –
this is a key benefit of Automatic Port Extensions!

Will using both an open and a short improve accuracy?

- Using two standards makes little difference for broadband applications, as many ripples occur and calculated loss is the same for open or short
- Using two standards improves accuracy for narrowband applications, where a full ripple cycle does not occur



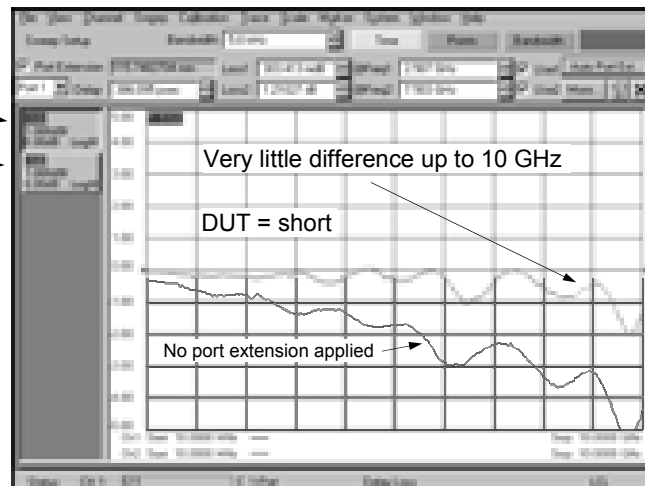
Broadband



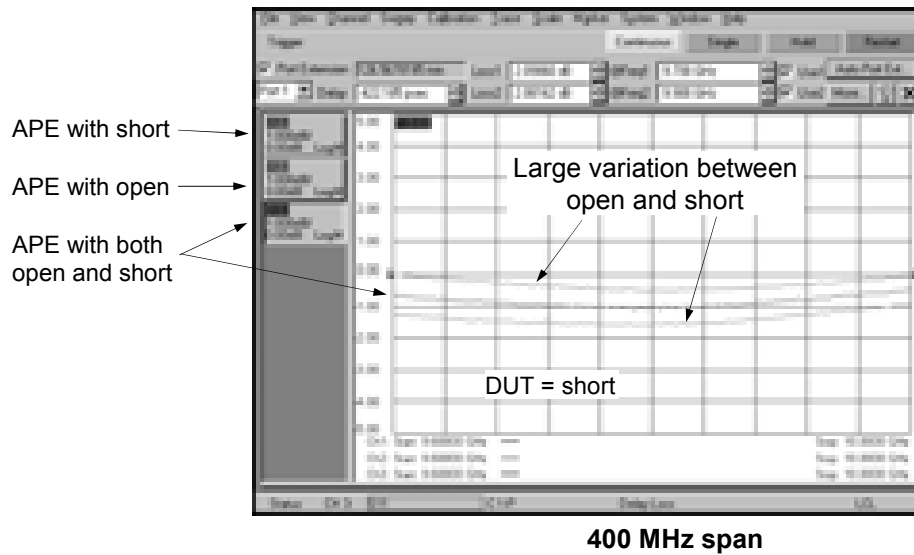
Broadband APE Example

APE with short

APE with open



Narrowband APE Example

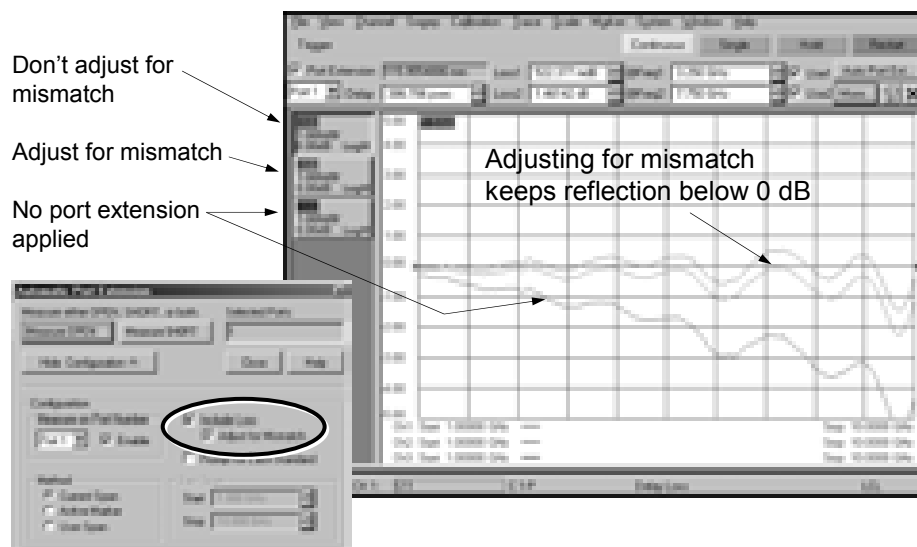


Page 81

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Feb. 23, 2006

Adjusting for Mismatch

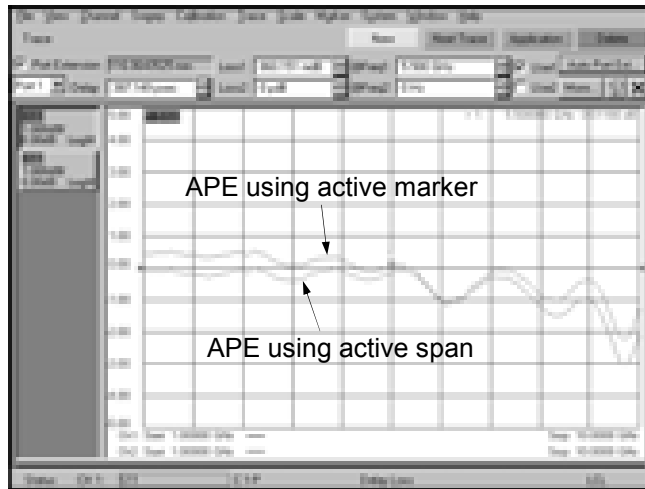


Page 82

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Active Span or Active Marker

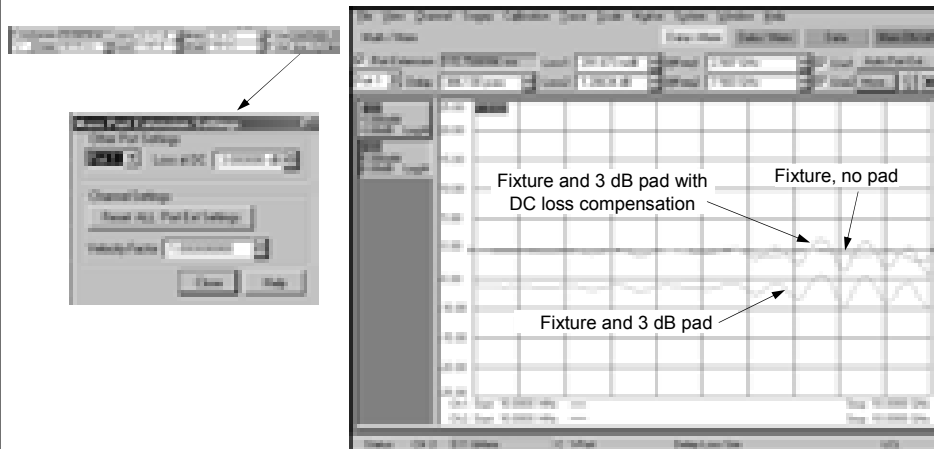


Note: when using active marker, selecting or not selecting "adjust for mismatch" makes no difference

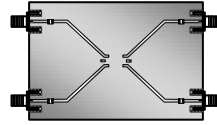
Loss at DC

Offsets the entire freq span to account for a fixed loss (e.g. 3 dB attenuator)

Use positive value to compensate for loss added after APE



Summary of Automatic Port Extensions



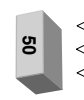
Ideal for in-fixture applications where complete calibration standards are not available

Eliminate the need to design and build difficult load standards

Applicable to a wide range of fixture designs

Works with probes too

Easy to use and quick to get results



Agenda

Overview of PNA FW Rev. 6.0

Application Code Version: A.06.00
Hard Disk Drive Version: S.05.40

Cal Registers

TRL Calibration with 4-port 20 GHz PNA-L

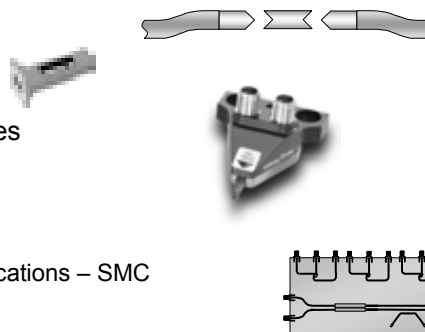
Unknown Thru Calibration

Offset Load Cal

Fixture And Probe Techniques

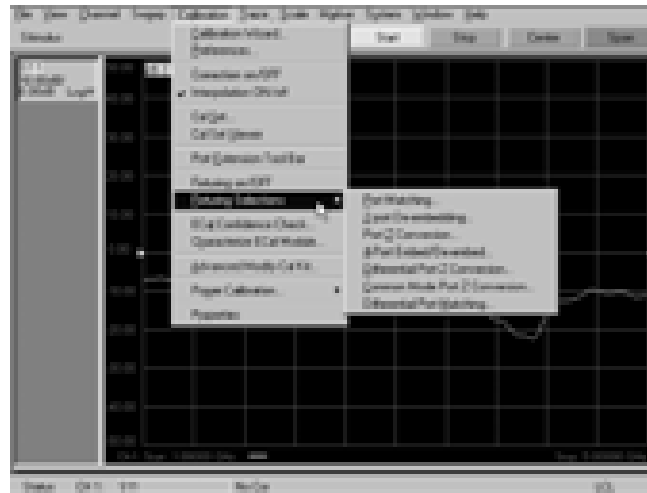
- Auto port extensions
-  • Embedding/de-embedding
- Frequency Converter Applications – SMC
- Measuring fixtures/probes

Q&A



Fixturing for the Masses

Fixturing features are same or similar to 4-port PNA-L, ENA, and PLTS



Page 87

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Feb. 23, 2006

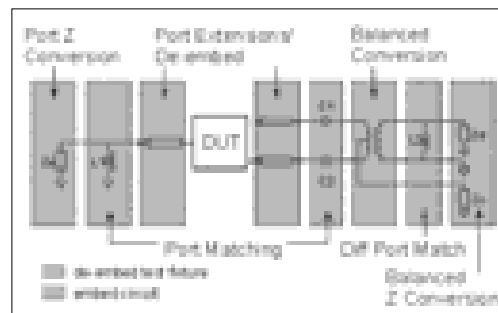
Order of Fixturing Operations

First, single-ended functions are processed in this order:

- Port extensions
- 2-port de-embedding
- Port Z (impedance) conversion
- Port matching / circuit embedding
- 4-port network embed/de-embed

Then, balanced functions are processed in this order:

- Balanced conversion
- Differential- / common-mode port Z conversion
- Differential matching / circuit embedding



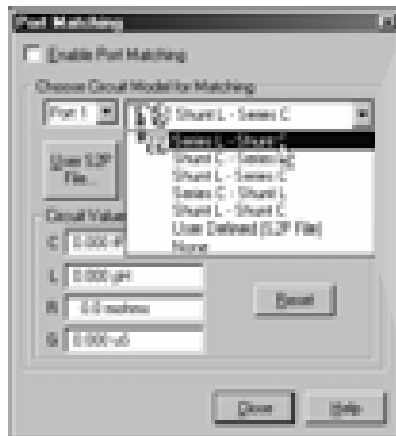
Example circuit simulation

Page 88

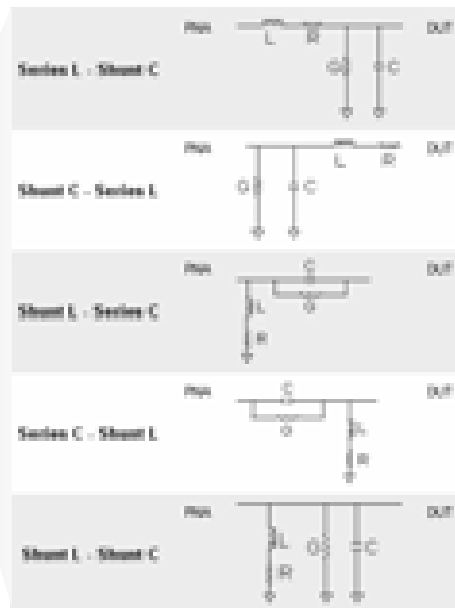
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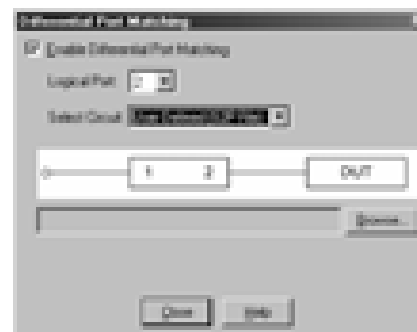
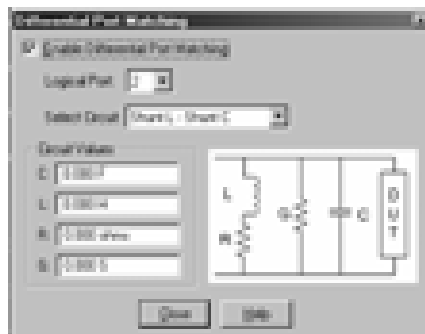
Port Matching



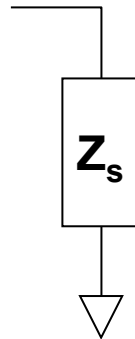
Port matching feature
is same as embedding



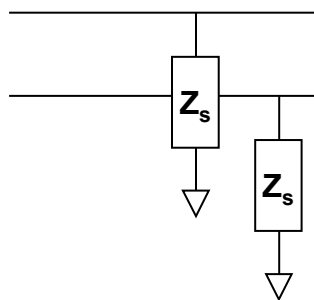
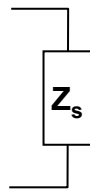
Differential Port Matching



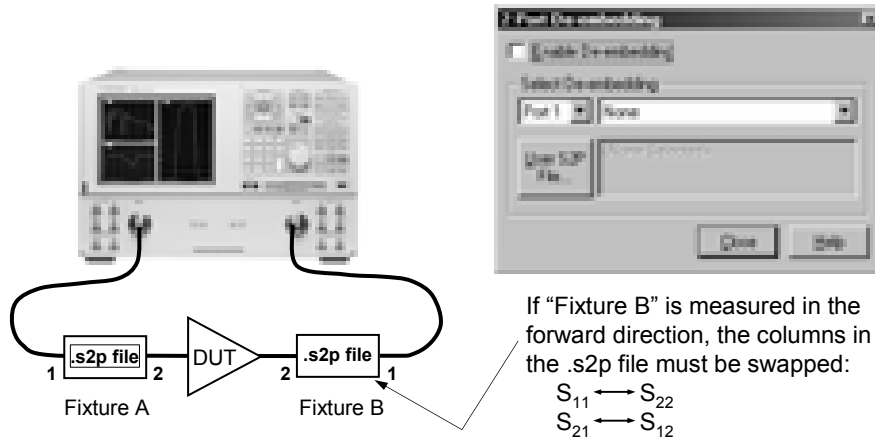
Port Z (Impedance) Conversion



Differential Port Z (Impedance) Conversion



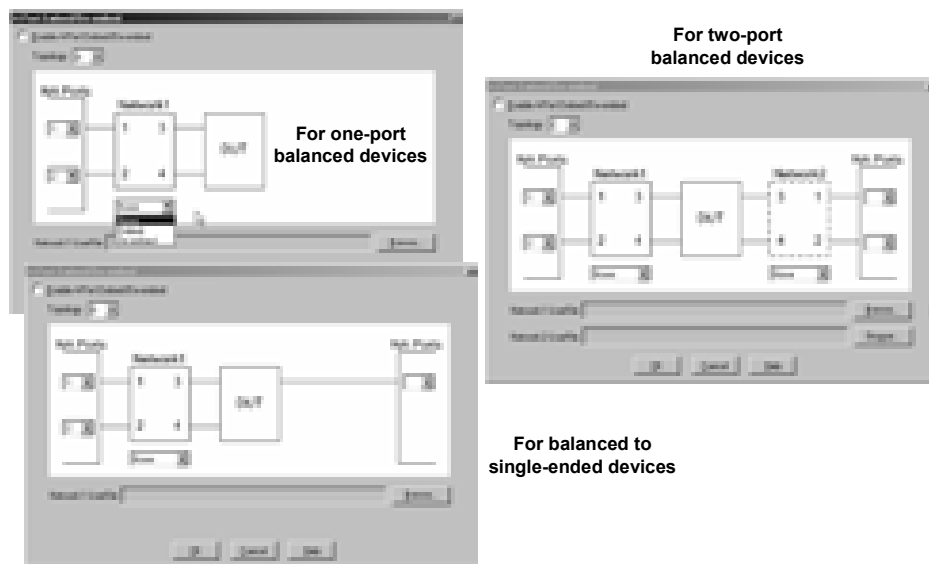
2-Port De-Embedding



In all cases, the assumption is:

- Port 1 of the fixture is connected to the PNA
- Port 2 of the fixture is connected to the DUT

4-Port Embedding/De-Embedding



Question: On a balanced port, what is the difference between:

Don't Forget to Turn Fixturing On!

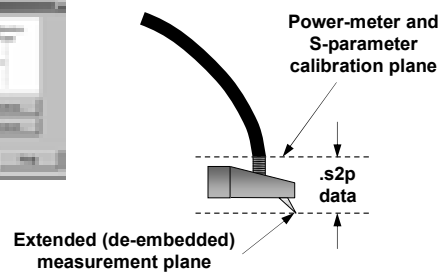
On-wafer SMC Measurements

Previous versions of FCA (Option 083) did not allow on-wafer measurements using Scalar Mixer Cal (SMC)

A.06.xx allows embedding of probe data files during SMC

Perform power-meter and S-parameter calibrations in coax

After coax calibrations, reference plane is at probe tip



Page 97

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Feb. 23, 2006

Agenda

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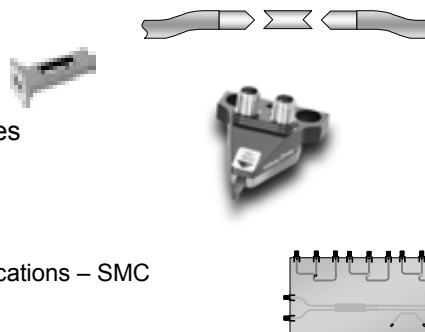
Offset Load Cal

Fixture And Probe Techniques

- Auto port extensions
- Embedding/de-embedding
- Frequency Converter Applications – SMC

- Measuring fixtures/probes

Q&A



Page 98

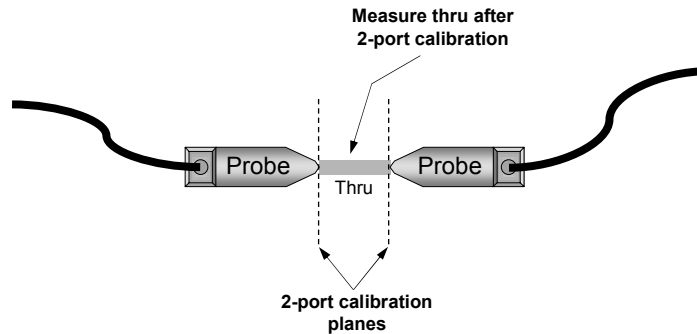
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How Do I Get My Probe De-Embedding Data?

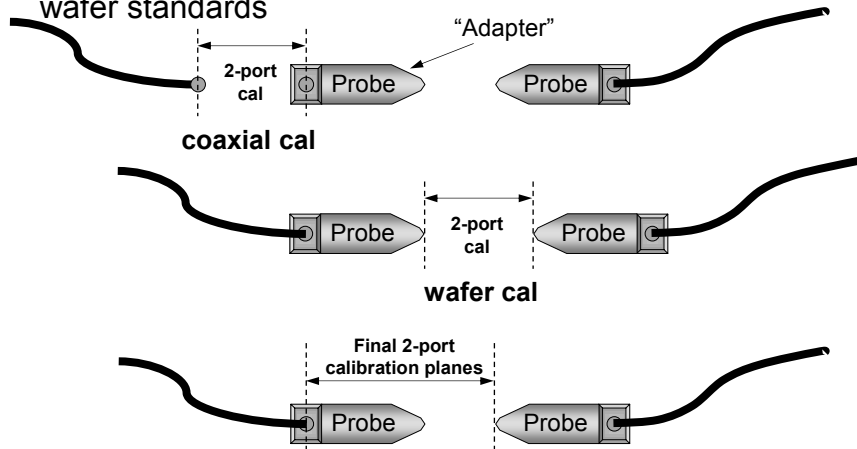
Perform an SOLT or TRL cal using wafer probes

Measure thru device and save data in .s2p file for de-embedding in later step



How Do I Get My Probe De-Embedding Data?

Perform an adapter removal calibration using coaxial and on-wafer standards



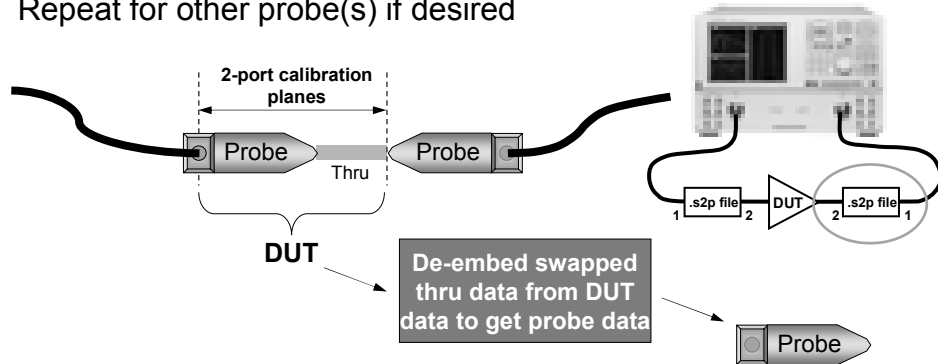
How Do I Get My Probe De-Embedding Data?

Measure thru plus probe

De-embed swapped thru data to obtain probe data

Save probe data in .s2p file for later use in measuring DUTs

Repeat for other probe(s) if desired



Page 101

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Alternate Way to Get Probe + Thru Data

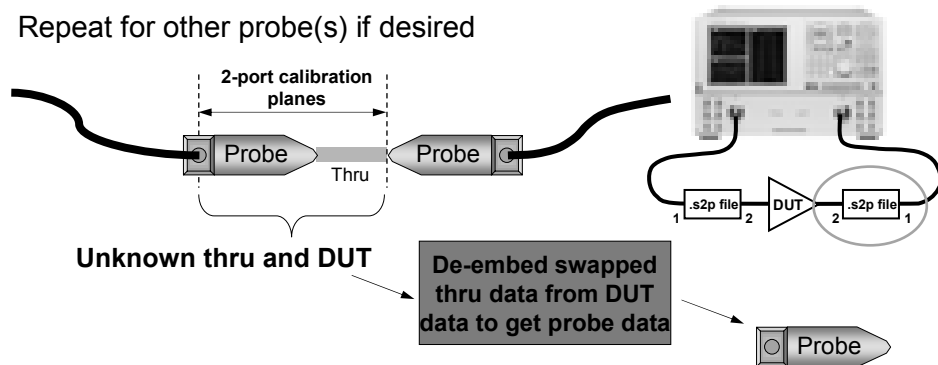
Perform unknown thru cal in coax and with probe

Measure thru plus probe

De-embed swapped thru data to obtain probe data

Save probe data in .s2p file for later use in measuring DUTs

Repeat for other probe(s) if desired



Page 102

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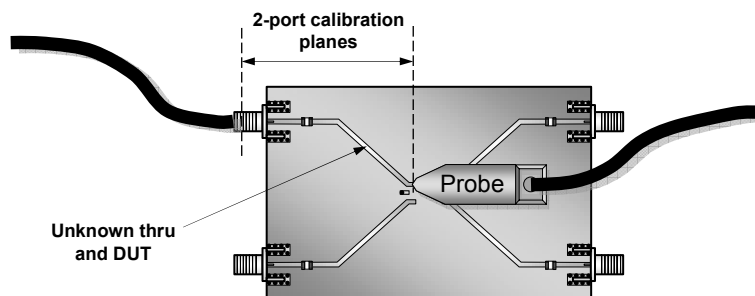
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How Do I Get My Fixture De-Embedding Data?

Perform an unknown thru cal using coax on one side, a probe on the other side, and the fixture itself for the unknown thru

Measure the fixture section and save data as .s2p file

Repeat for each section of fixture



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台灣安捷倫科技股份有限公司

台北市104 復興南路一段2 號8 樓
電話：(02) 8772-5888

桃園縣平鎮市324 高雙路20 號
電話：(03) 492-9666

台中市408 台中市文心路一段552號12C
電話：(04) 2310-6915

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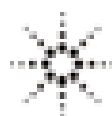
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